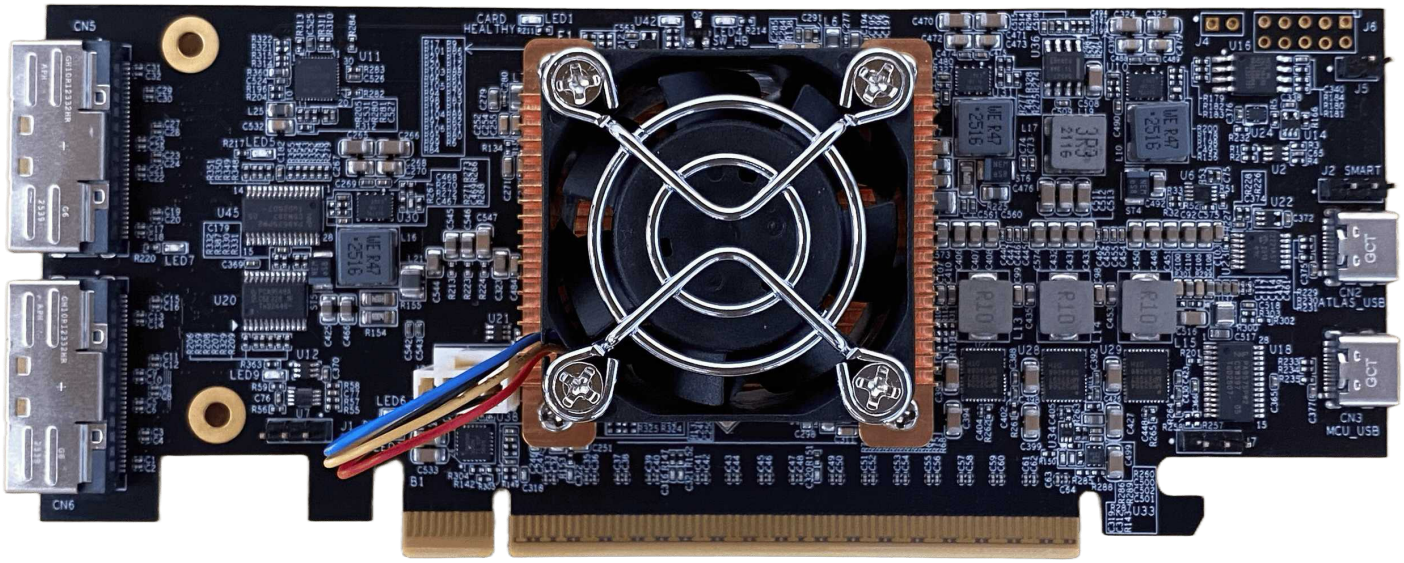
SERIAL CABLES

PCIe 6.0 CDFP HHHL Host Card

w/ Broadcom Atlas III 32-Lane Switch

TECHNICAL MANUAL



Revision 1.1 Nov 2026

PCI6-AD-x16HI-BG6-32

Command-line interface for monitoring

PCI EXPRESS 6.0

Serial Cables LLC.

Phone: (303) 495-2320 Email: sales@serialcables.com https://serialcables.com

Table of Contents

Declaration and Revision Notice **3**
Product Overview **4**
Safety, Handling, and Compliance **5**
Electrical Safety 5
ESD Protection 5
Thermal and Airflow Considerations 5
Compliance 5
Hardware Specifications **6**
Connector Locations and Functions 7
Port and Station Mapping 9
LED Indicators 10
Practical Applications and System Integration **12**
Gen 6 JBOF Connectivity 12
Direct-Attached EDSFF SSDs 12
PCIe Gen 6 Slot Expansion 14
Command-Line Interface (CLI) Setup **15**
Connection Steps 15
CLI Command Reference **16**
Command Usage Notes **17**
Firmware Upgrade and Management – fdl 17
System Diagnostics – lsd 19
Register Write – mw 19
Switch Register Dump – dr 20
Port Register Dump – dp 21
Flash Dump — df 21
Connector Reset — conrst 22
Port Link Status— showport 23
Built-In Self-Test — bist 24
Host Card Mode Configuration — setmode 25
Show Host Card Mode — showmode 25
PCIe Clock Spread Setting — spread 26
PCIe Clock Output Control – clk 26
SDB Port Control — sdb 27
UART Path Selection — uart 27
Power Status — pwr 28
Port Error Counters — counters 29
FLIT Mode Control — flit 29
SMBus Read — iicwr 30
SMBus Write — iicw 30
Bifurcation Mode Programming — bifmode 31
Link Training Status — ltssm 32

PCIe FLIT Diagnostics — flitdiag 33
PCIe Link Speed Control — speed 34
MCTP Command – mctp 35
MCTP Packet – packet 35
System Version — ver 36
System Information — sysinfo 37
System Reset — reset 38
Maintenance and Diagnostics **39**
Revision History **40**
Contact Us **40**

Declaration and Revision Notice

Serial Cables, Inc. reserves the right to modify the design, specifications, software, or documentation of the product described in this manual at any time without prior notice.

This product – including all related software, firmware, and documentation – is the property of Serial Cables, Inc. and/or its licensors. It is provided under license and may be used or reproduced only in accordance with the terms of that license. No part of this document may be copied, reproduced, or distributed in any form without prior written permission from Serial Cables, Inc.

Product manuals may be periodically revised to reflect hardware, firmware, or mechanical updates. For the most recent documentation and software releases, please visit **https://serialcables.com/**.

Product Overview

The Serial Cables **Atlas3 32-A0 Host Adapter Card** (PCI6-AD-x16HI-BG6-32) is a PCIe Gen 6 adapter built around the **Broadcom PEX90032 Atlas3 switch**. Supporting up to 32 PCIe lanes, the card connects a host system to external PCIe devices through two MCIO x8 connectors. The adapter uses a PCIe x16 host interface and supports flexible downstream port configurations.

The adapter supports both managed and unmanaged operating modes. An onboard microcontroller provides command-line interface (CLI) functionality for switch configuration, device management, diagnostics, and firmware updates. Additional capabilities include non-transparent port support, DMA channels, peer-to-peer data transfers, and PCIe hot-plug functionality.



Key Features

- **PCIe Gen 6 performance** – Broadcom PEX90032 switch supporting up to 32 lanes and 16 ports.
- **Flexible connectivity** – Two right-angle MCIO x8 connectors (SFF-TA-1016) and a PCIe x16 host interface.
- **PCIe Gen 6 capabilities** – Supports FLIT mode and Forward Error Correction (FEC).
- **Managed and unmanaged operation** – Supports firmware-based management and operation without managed firmware.
- **Advanced PCIe functionality** – Non-transparent ports, DMA channels, peer-to-peer transfers, and hot-plug support.
- **Integrated management** – Onboard microcontroller with CLI access for configuration, diagnostics, and firmware updates.

Safety, Handling, and Compliance

The Atlas3 32-A0 Host Adapter Card should be installed and handled using standard PCIe hardware and ESD-safe procedures. Follow the precautions below when installing, configuring, or servicing the card.

Electrical Safety

- Power down the host system and disconnect external power before installing or removing the card.
- Do not connect or disconnect PCIe cables while the system is energized.
- Inspect the card, cables, and connectors for damage before installation.
- Use compatible PCIe cables and connectors with the correct pin assignments for the intended application.

ESD Protection

- Work in an ESD-safe area using a grounded mat and wrist strap.
- Keep the card in antistatic packaging until installation.
- Avoid touching connector contacts, exposed traces, or component leads.

Thermal and Airflow Considerations

- Maintain adequate airflow around the Broadcom PEX90032 switch and its cooling assembly.
- Keep ventilation paths unobstructed during operation.
- Operate the card within its specified temperature range of 0°C to +40°C.

Compliance

This product should be installed and operated in accordance with applicable electrical safety and electromagnetic compatibility (EMC) requirements.

Hardware Specifications

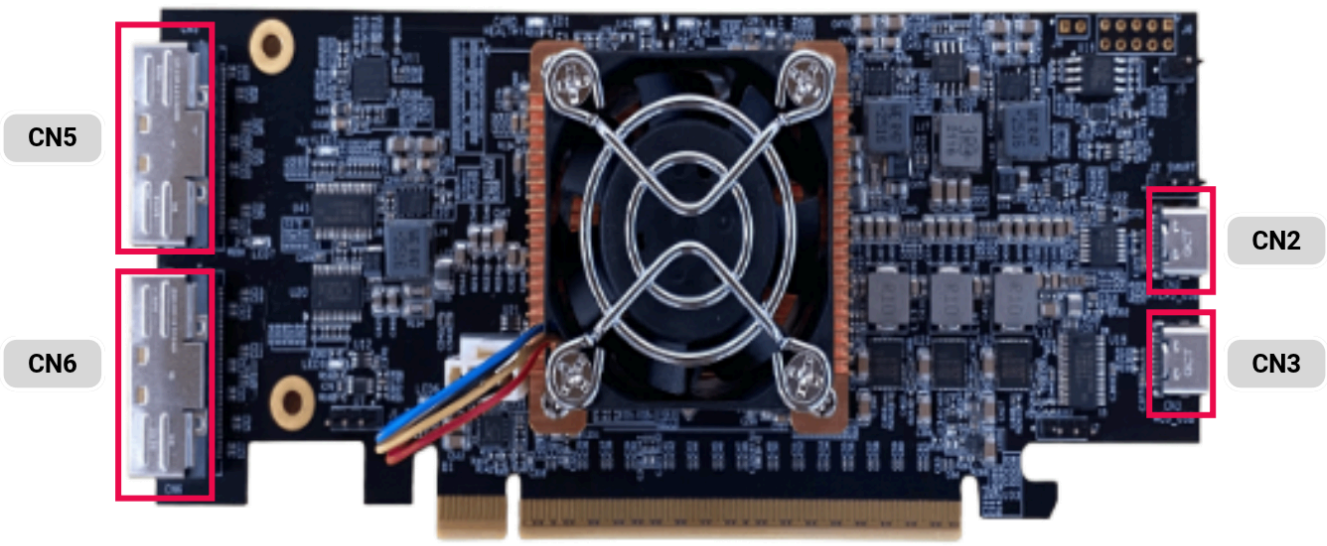
The Atlas3 32-A0 Host Adapter Card uses the Broadcom PEX90032 PCIe Gen 6 switch to provide high-speed connectivity between a host system and external PCIe devices. The card supports up to 32 PCIe lanes, with two MCIO x8 connectors for downstream connections.

Parameter	Specification
Part Number	PCI6-AD-x16HI-BG6-32
PCIe Switch	Broadcom Atlas3 PEX90032
PCIe Generation	PCIe Gen 6
PCIe Lanes	Up to 32 lanes
PCIe Ports	Up to 16 ports
Operating Modes	Managed and unmanaged
MCIO Connectors	2 × right-angle MCIO x8 (SFF-TA-1016)
PCIe Interface	PCIe x16 edge connector (golden finger)
Management Interfaces	2 × USB Type-C connectors for Atlas3 debug/UART and onboard MCU access
Maximum Power Consumption	55 W (Gen 6 x32 links)
Operating Temperature	0°C to +40°C
PCB Dimensions	167 × 69 × 44 mm (L × H × T), including heatsink

Connector Locations and Functions

The connector designators are silk-screened on the PCB. CN5 and CN6 provide downstream PCIe connections, while CN2 and CN3 provide switch debug and MCU management access.

Designator	Connector Type	Function / Description
CN2	USB Type-C	Atlas3 I²C slave interface and selectable SDB/SMART UART access; two COM ports.
CN3	USB Type-C	Primary MCU command-line interface for configuration, diagnostics, and firmware updates.
CN5	MCIO x8 (SFF-TA-1016)	Routes PCIe lanes 8–15 to downstream devices; includes clock, I²C, and PERST# sideband signals.
CN6	MCIO x8 (SFF-TA-1016)	Routes PCIe lanes 0–7 to downstream devices; includes clock, I²C, and PERST# sideband signals.



CN2 – USB Type-C Connector

CN2 exposes two USB serial interfaces. The first connects to the Atlas3 I²C slave interface, while the second can be switched between SDB and SMART UART. The I²C slave and SMART UART functions require managed firmware support.

CN5 and CN6 – MCIO x8 Connectors

CN5 and CN6 each provide eight PCIe Gen 6 lanes for downstream devices. CN5 routes lanes 8–15 and CN6 routes lanes 0–7. Both connectors provide the following sideband signals:

- **Reference Clocks** – Four dedicated PCIe HCSL clock outputs at pins A8/A9, A11/A12, A26/A27, and A29/A30.

- **I²C Interfaces** – Two dedicated interfaces at pins B8/B9 and B26/B27.
- **Reset Signals** – Four PERST# signals at pins B11, B12, B29, and B30.

The following tables show the PCIe lane and sideband pin assignments for **CN6**:

	2	3	5	6	8	9
A	PERN7	PERP7	PERP6	PERN6	MCIO_CLKA_P0	MCIO_CLKA_N0
B	PETN7	PETP7	PETP6	PETN6	MCIO_SCL_A0	MCIO_SDA_A0
	14	**15**	**17**	**18**	**11**	**12**
A	PERN5	PERP5	PERP4	PERN4	MCIO_CLKA_P1	MCIO_CLKA_N1
B	PETN5	PETP5	PETP4	PETN4	MCIO_PERST#_A0	MCIO_PERST#_A1

	20	21	23	24	26	27
A	PERN3	PERP3	PERP2	PERN2	MCIO_CLKB_P0	MCIO_CLKB_N0
B	PETN3	PETP3	PETP2	PETN2	MCIO_SCL_A0	MCIO_SDA_A0
	32	**33**	**35**	**36**	**29**	**30**
A	PERN1	PERP1	PERP0	PERN0	MCIO_CLKB_P1	MCIO_CLKB_N1
B	PETN1	PETP1	PETP0	PETN0	MCIO_PERST#_B0	MCIO_PERST#_B1

CN5 uses the same pin arrangement, with lane assignments 8–15.

CN3 – USB Type-C Connector

CN3 connects to the onboard microcontroller (MCU) and provides the primary command-line interface for firmware updates, switch configuration, diagnostics, and troubleshooting.

Port and Station Mapping

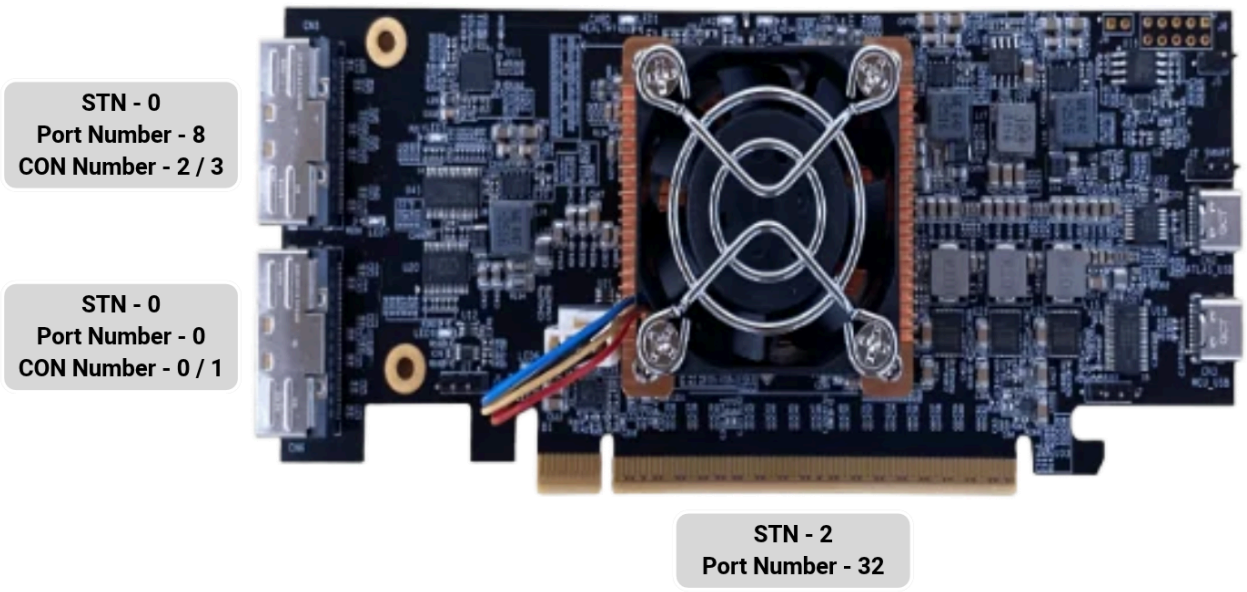
The Broadcom PEX90032 uses two active stations, each supporting up to 16 PCIe lanes:

- **Station 0** connects to the two MCIO connectors through ports 0 and 8.
- **Station 2** connects to the PCIe x16 host interface through port 32.

Each MCIO connector also has two Connector (CON) numbers used to identify its associated I²C and reset paths in CLI commands such as **conrst**, **iicw**, and **iicwr**.

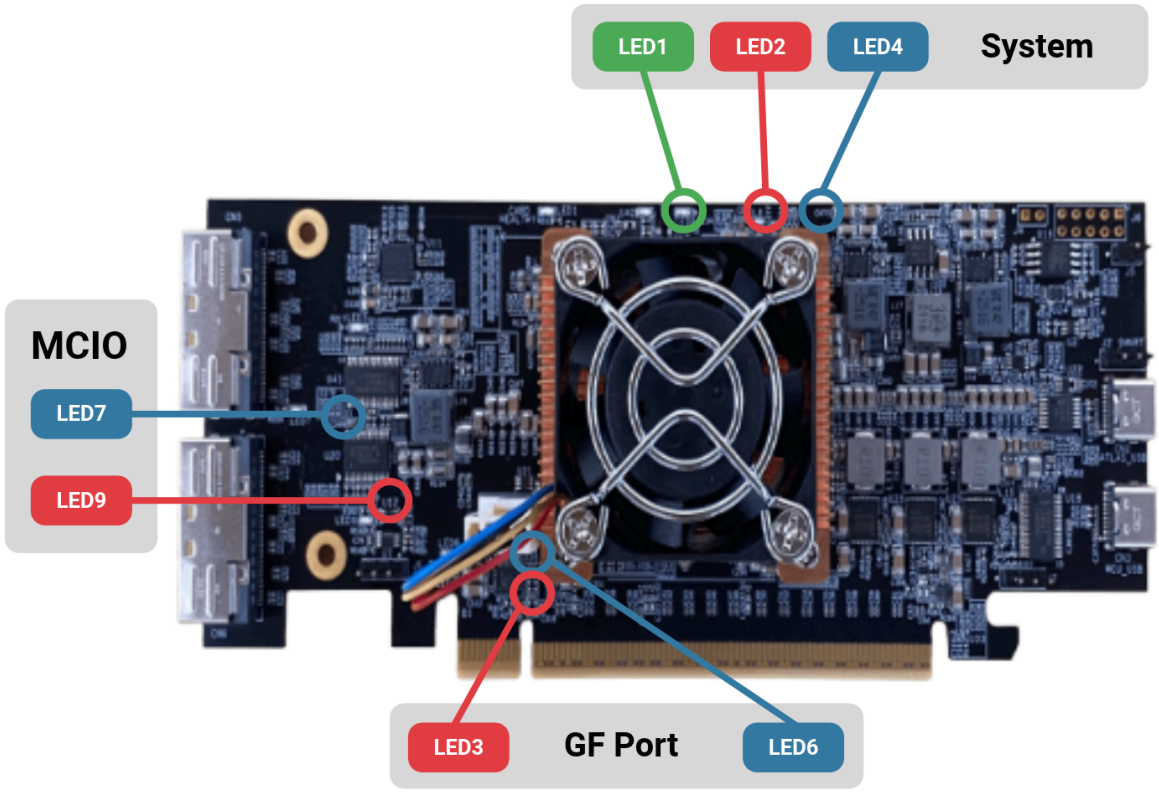
The mapping below identifies the station, port, and CON assignments for the host adapter:

Interface	Station	Port Number	CON Number
MCIO CN6 (lower)	0	0	0 / 1
MCIO CN5 (upper)	0	8	2 / 3
PCIe Golden Finger	2	32	N/A



LED Indicators

The Atlas3 32-A0 includes system-status, PCIe link-speed, and link-width LEDs. Their locations are identified in the board illustration.



System Status LEDs

LED ID	Color	Description
LED2	Red	**System Error Indicator.** Turns on for: • Second expiration of the watchdog timer • Built-In Self-Repair (BISR) error • Firmware signature authentication failure • Double-bit ECC errors
LED4	Blue	**Atlas3 Heartbeat.** Blinks when managed firmware is running normally. Remains solid on when unmanaged firmware is loaded.
LED1	Green	**MCU Status.** Blinks when the MCU firmware is active and responding.

Link Speed LEDs

The blue Link Speed LEDs indicate the negotiated PCIe generation for the host interface and MCIO link:

- **Active link** — The LED blink rate corresponds to the negotiated PCIe generation.
- **Gen6 link** — The corresponding LED remains solid.
- **Detailed link status** — Use the **showport** CLI command to view negotiated speed and width.

LED ID	Location	Color
LED6	PCIe Golden Finger	**Blue**
LED7	MCIO connectors	**Blue**

The blink rate identifies the negotiated PCIe generation, with faster blinking indicating higher link speeds. At Gen 6, the LED remains steadily lit. The table below shows the LED behavior for each generation:

PCIe Generation	Link Speed LED
Gen 1 (2.5 GT/s)	0.25 Hz
Gen 2 (5.0 GT/s)	0.5 Hz
Gen 3 (8.0 GT/s)	1 Hz
Gen 4 (16.0 GT/s)	2 Hz
Gen 5 (32.0 GT/s)	4 Hz
Gen 6 (64.0 GT/s)	Steady on

Link Width LEDs

The red Link Width LEDs indicate whether the negotiated link width matches a supported configuration. LED3 remains off when the host link negotiates x16, while LED9 remains off when the MCIO links negotiate a supported configuration: one 16-lane link, two 8-lane links, four 4-lane links, or eight 2-lane links.

LED ID	Monitored Port	Color
LED3	PCIe Golden Finger	**Red**
LED9	MCIO connectors	**Red**

Use **showport** for the negotiated link speed and width, including links reported as Active, Idle, or Degraded.

- A **Degraded** status indicates that the negotiated link speed or width does not match the desired configuration.

Practical Applications and System Integration

The Atlas3 32-A0 provides two MCIO x8 interfaces for connecting external NVMe storage and PCIe expansion hardware. Each interface supports up to eight PCIe lanes, allowing the card to distribute 16 downstream lanes across compatible devices.

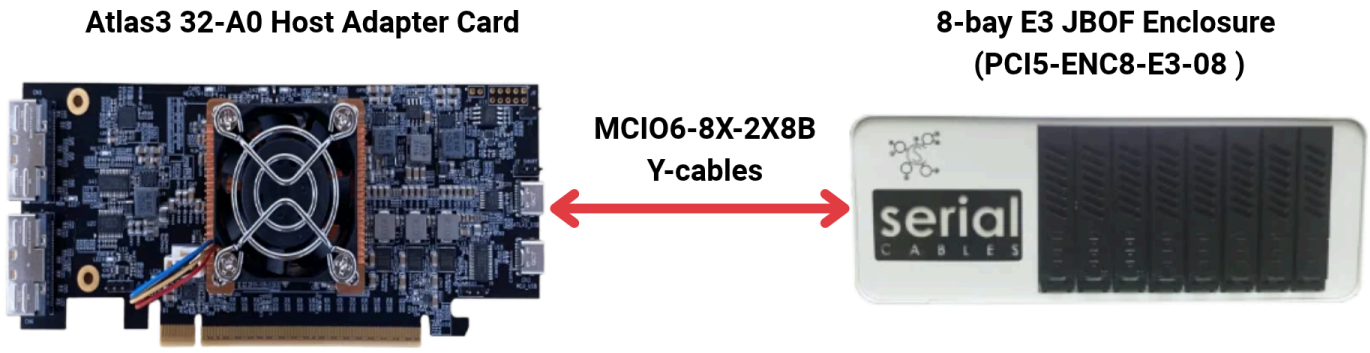
The following configurations illustrate common applications using Serial Cables enclosures, adapters, and cable assemblies:

Gen 6 JBOF Connectivity

Connect the Atlas3 32-A0 to the Serial Cables PCI5-ENC8-E3-08 eight-bay E3 JBOF enclosure using **MCIO6-8X-2X8B Y-cables**. Each cable divides one MCIO x8 connection into two x4 connections, providing four x4 connections across both host adapter ports.

The number of accessible drives depends on the enclosure's internal routing and the configured PCIe lane allocation.

Component	Description
Host Adapter	Atlas3 32-A0 Host Adapter Card (this product)
Cabling	MCIO6-8X-2X8B Y-cables
Target System	PCI5-ENC8-E3-08 8-bay E3 JBOF enclosure
Storage Devices	Compatible E3 SSDs



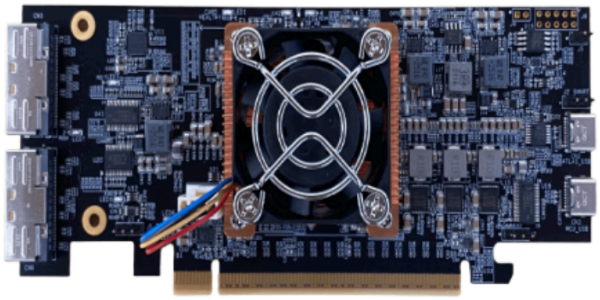
Direct-Attached EDSFF SSDs

Use the **MCIO6-8X-EDSFFX2-1X4 breakout cable** to connect two EDSFF SSDs to a single MCIO x8 port. Each drive receives a dedicated x4 PCIe connection, allowing up to four drives across both ports.

Compatible EDSFF devices may include E1.S, E1.L, E2, and E3 SSDs, depending on connector compatibility and power requirements.

Component	Description
Host Adapter	Atlas3 32-A0 Host Adapter Card (this product)
Cabling	MCIO6-8X-EDSFFX2-1X4 cable
Target Devices	Compatible E1.S, E1.L, E2, or E3 SSDs

Atlas3 32-A0 Host Adapter Card



MCIO6-8X-EDSFFX2-1X4 Breakout Cable



EDSFF SSDs

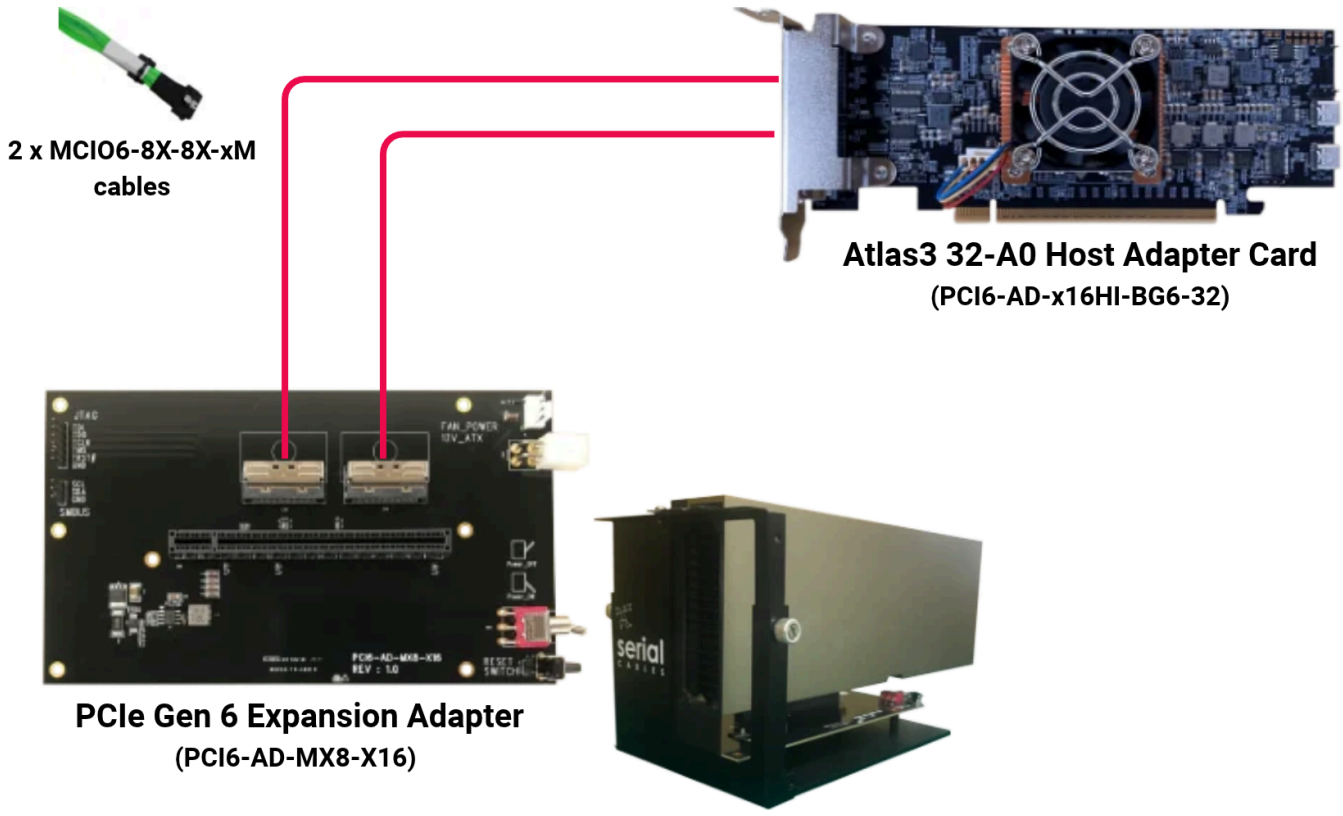


PCIe Gen 6 Slot Expansion

The Atlas3 32-A0 supports external PCIe add-in-card testing using the PCI6-AD-MX8-X16 expansion adapter. Two **MCIO6-8X-8X-xM** cables connect the host adapter's MCIO x8 ports to the expansion adapter's two MCIO inputs.

This configuration provides a physical PCIe x16 slot using the host adapter's 16 downstream lanes.

Component	Description
Host Adapter	Atlas3 32-A0 Host Adapter Card (this product)
Cabling	MCIO6-8X-8X-xM cables
Expansion Adapter	PCI6-AD-MX8-X16 adapter
Target Devices	Compatible PCIe add-in cards



Command-Line Interface (CLI) Setup

The Atlas3 32-A0 Host Adapter Card includes an onboard microcontroller (MCU) that provides command-line access for switch configuration and diagnostics, as well as firmware management. The card includes two USB Type-C interfaces:

- **CN3** — Primary interface for MCU CLI access and firmware updates.
- **CN2** — Provides Atlas3 I²C slave and selectable SDB/SMART UART access. It is not used for the standard MCU CLI.

The CLI can be used to:

- Monitor temperature, critical voltages, fan speed, power consumption, and PCIe link status.
- Access switch and port registers for configuration and troubleshooting.
- Manage Atlas3 and MCU firmware updates.
- Control PCIe reference clocks and connector reset signals.
- Run board-level diagnostics

Connection Steps

1. Connect a USB Type-C cable between the host computer and **CN3** on the Atlas3 32-A0 Host Adapter Card.

2. After the USB connection is detected, identify the assigned COM port using your system's Device Manager.

3. Open your serial terminal software (Tera Term, PuTTY, or equivalent) and connect to the assigned COM port.

4. A successful serial connection displays the MCU command prompt.

CLI Command Reference

Commands	Description
fdl	Updates unmanaged switch SBR images, managed firmware, MCU firmware, or a multi-config SBR bundle
lsd	Displays temperature, critical voltages, fan speeds, and board power consumption
mw	Writes a 32-bit value to a specified register within the Atlas3 switch
dr	Dump switch-level registers for diagnostic or debugging purposes
dp	Dumps port-specific switch registers for the selected port
df	Dumps contents of the switch's onboard flash memory
conrst	Sends a 300 ms PERST# pulse to selected downstream MCIO connectors
showport	Displays link status and connection details for USP/DSP ports
bist	Runs the onboard Built-In Self-Test (BIST) for device diagnostics
setmode	Selects a preloaded SBR profile for MCIO bifurcation and Gen 6 precoding (hardware revision 1.1+)
showmode	Displays the active host-card mode
spread	Configures the PCIe clock spread spectrum setting
clk	Enables or disables the PCIe clock output
sdb	Sets the MCU SDB port state (on/off)
uart	Selects CN2 UART routing between SMART UART and Atlas3 SDB
pwr	Displays the status of the onboard power regulators
counters	Displays error counters and statistics for all active ports
flit	Configures PCIe Gen 6 FLIT mode settings
iicwr	Performs an I²C/SMBus write-read transaction
iicw	Performs an I²C/SMBus write transaction
bifmode	Changes bifurcation mode by programming an SBR from MCU QSPI to switch flash.
ltssm	Reports LTSSM state or continuously monitors PCIe link training.
flitdiag	Displays PCIe Gen 6 FLIT diagnostics, including error and BER information.
speed	Queries or configures PCIe target link speed and initiates retraining.
mctp	Executes Management Component Transport Protocol (MCTP) commands
packet	Executes packet-related operations
ver	Displays version information for the host card, MCU firmware, and Atlas3 firmware
sysinfo	Displays system configuration, firmware information, power status, PCIe link state, and onboard diagnostics
reset	Performs reset operations for the onboard MCU, PCIe hierarchy, or Atlas3 switch

Command Usage Notes

Firmware Upgrade and Management – fdl

The **fdl** command transfers firmware images using XMODEM. It supports unmanaged mini and main SBR images, managed switch firmware, MCU firmware, and a multi-configuration SBR bundle stored in MCU QSPI flash.

Enter **fdl** followed by one of the following modes:

- **mini** – Updates the unmanaged mini SBR firmware.
- **main** – Updates the unmanaged main SBR firmware.
- **fw** – Updates the managed switch firmware.
- **mcu** – Updates the onboard MCU firmware.
- **config** – Uploads the multi-configuration SBR bundle to MCU QSPI flash.

When executed, the system prompts for confirmation before erasing and writing flash memory.
Press **Y** to continue or **Ctrl+X** to cancel.

The **mini**, **main**, and **fw** commands erase all regions of the Atlas3 switch flash before the new firmware is written.

Firmware Upload Procedure

Step 1 – Connect via Serial Interface

- Connect a USB-C cable to CN3 on the host adapter.
- Identify the COM port in your system's **Device Manager**.
- Open a terminal emulator such as **TeraTerm/puTTy** (Windows) or **minicom** (Linux) and connect to that COM port.
- A successful connection will display the command prompt (Cmd>).

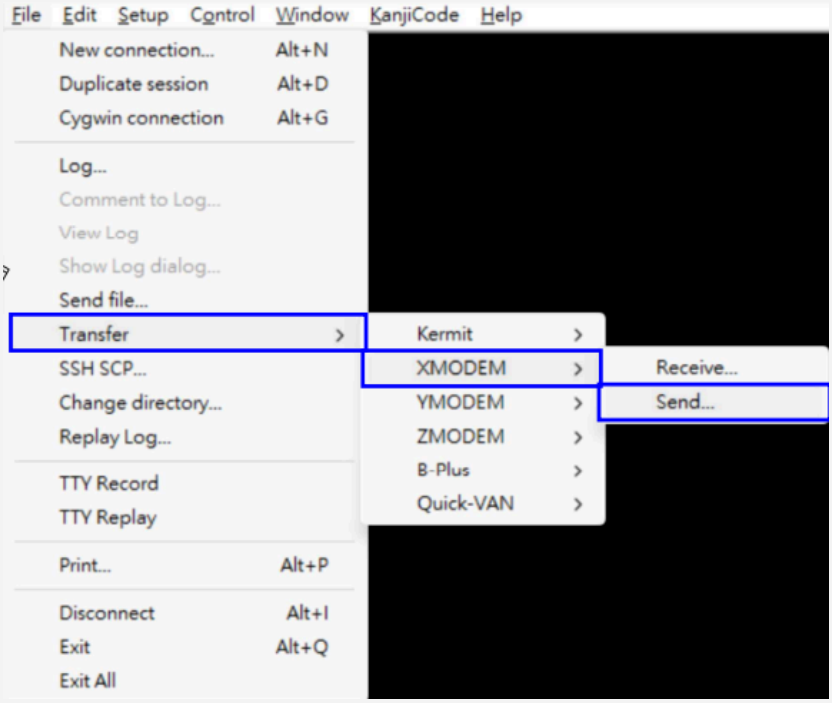
Step 2 – Run the Upload Command

1. Enter the appropriate **fdl** command (e.g., **fdl main**).
2. When prompted, press **Y** to confirm the upgrade or **Ctrl+X** to cancel.
3. The selected firmware storage is prepared, and the system waits for the XMODEM transfer. The mini, main, and fw modes erase the Atlas3 switch flash regions.

Continued on the next page.

Step 3 – Send the Firmware File via XMODEM

- In **TeraTerm** – Go to **File** → **Transfer** → **XMODEM** → **Send**, then select the **BIN firmware file**.



- In **minicom** – Use **Send File** → **XMODEM** and choose the **BIN firmware file**.

Step 4 – Apply the New Firmware

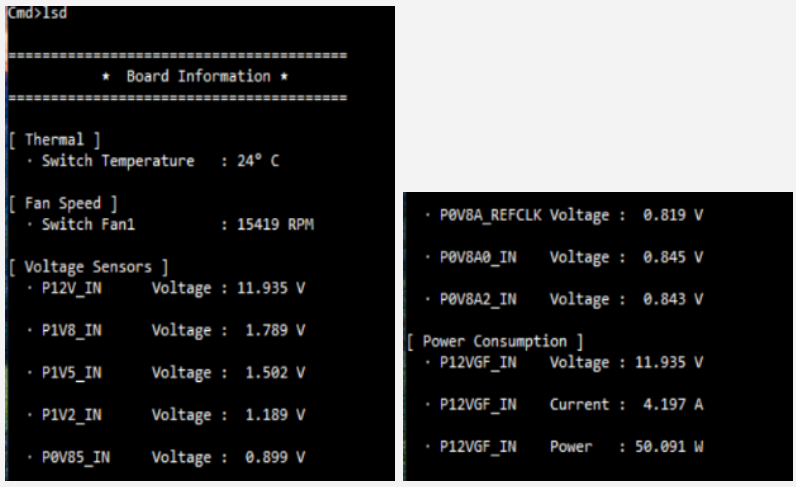
- After the upload finishes, power cycle the host card for unmanaged or managed firmware updates. For MCU firmware upgrades, use the **reset** command instead of a power cycle to activate the new MCU firmware.

System Diagnostics – lsd

The **lsd** command displays board telemetry, including temperature near the Atlas3 switch, cooling-fan speed (RPM), monitored onboard voltages, and measured power consumption.

The output includes:

- **Thermal** – Reports the temperature near the Atlas3 PCIe switch.
- **Fan Speed** – Shows the host card fan RPM
- **Voltage Sensors –** Displays monitored critical voltages on the adapter.
- **Power Consumption** – Displays board input voltage, current, and calculated power.



Register Write – mw

The **mw** command writes a 32-bit value to a specific register address within the Atlas3 PCIe switch. It writes the specified hexadecimal data directly to the target register for switch configuration and low-level hardware control.

Enter the command **mw** followed by the register address (hex) and the data value (hex) to be written. Valid register addresses range from **0x00000000** to **0xFFFFFFFC**, and writable data values range from **0x00000000** to **0xFFFFFFFF**. For example:

- **mw fff0017c ffffffff** – This writes the data **0xFFFFFFFF** to the register address **0xFFF0017C** on the Atlas3 switch

Switch Register Dump – dr

The **dr** command reads and dumps switch-wide register values from the Atlas3 PCIe switch.
It retrieves low-level register data across the switch's address space for debugging, validation, and hardware bring-up.

Enter the command **dr** followed by the starting register address (hex) and an optional count (hex) to specify how many bytes to read. The valid register addresses and count values range from **0x00000000** to **0xFFFFFFFC**. For example:

- **dr 60800000** – Dumps switch registers beginning at 0x60800000 (MCIO port 0).

Register Address Mapping

Port register blocks use an offset of 0x8000. The MCIO Port 0 block begins at 0x60800000; host interface Port 32 begins at 0x60900000.

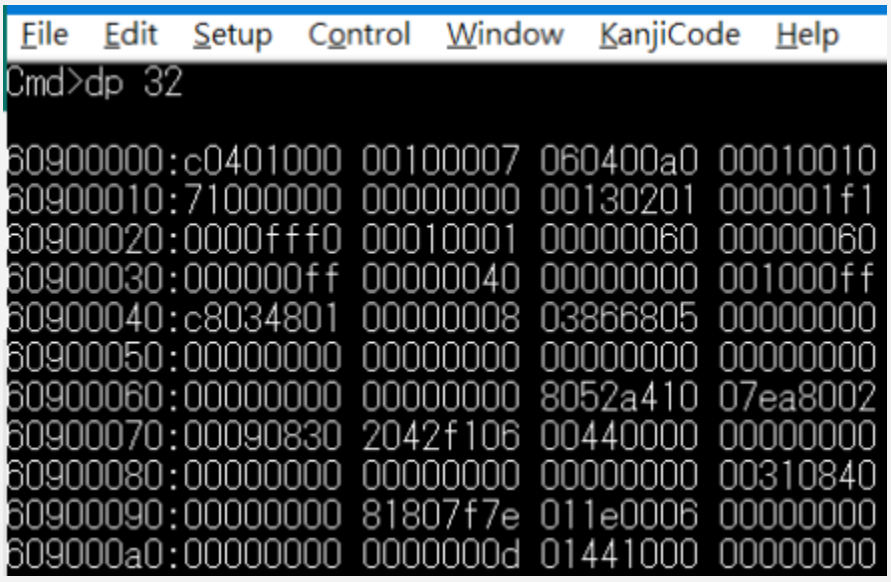
Interface	Port	Base Address
MCIO CN6 (lower)	0	0x60800000
MCIO CN5 (upper)	8	0x60840000
PCIe Golden Finger	32	0x60900000

Port Register Dump – dp

The **dp** command reads and dumps port-specific register values from the Atlas3 PCIe switch.
It displays low-level hardware data for a selected physical port and is primarily used for port-level debugging and validation.

Enter **dp** followed by a port number in the supported range 0–47 to dump the selected port's registers. For example:

- **dp 32** – Dumps switch register values for Port 32.



Refer to **Port and Station Mapping** for physical port assignments.

Flash Dump — df

The **df** command reads and dumps the contents of the switch flash memory to the console or a connected host interface. It retrieves raw flash data for firmware inspection, debugging, or verification.

Enter the command **df** followed by the start address (hex) and optionally the byte count (hex) to dump data from the switch flash memory. Both the address and count can range from 0x00000000 to 0xFFFFFFFC. For example:

- **df 400** – Dumps the flash contents starting from address 0x00000400
- **df 400 4** – Dumps 4 bytes of flash data starting from address 0x00000400

Connector Reset — conrst

The **conrst** command pulses the PERST# reset signal for a selected downstream MCIO connector or all connectors. Each pulse lasts 300 ms.

Enter **conrst** followed by a connector number (0–3) or all, and optionally a channel identifier. For example:

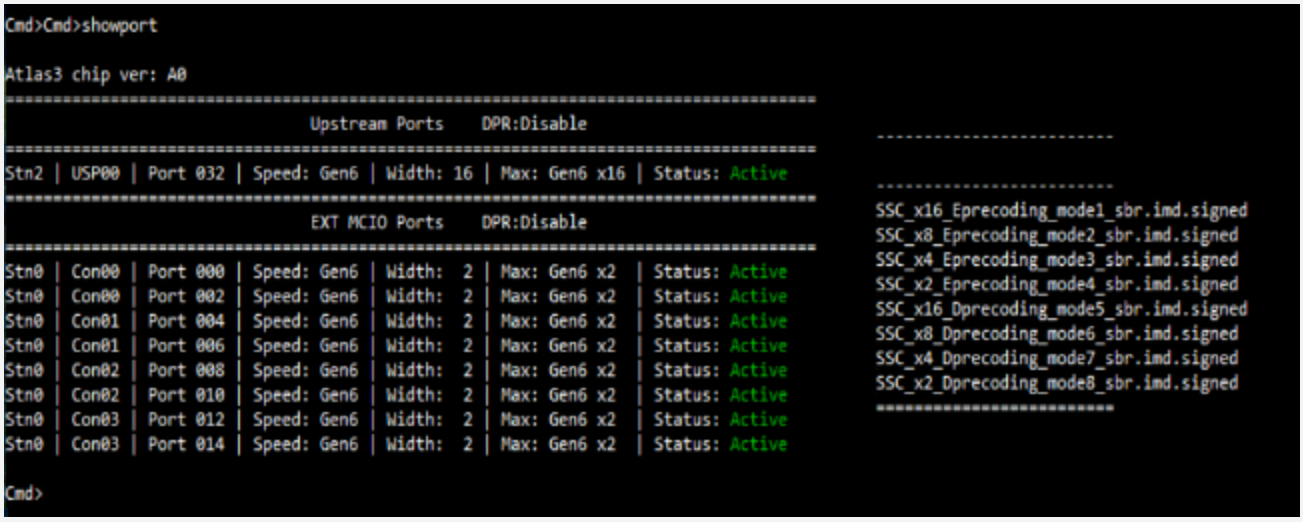
- **conrst 1** — Sends a PERST# reset to connector 1
- **conrst all** — Pulses the downstream MCIO reset lines.
- **conrst all a** — Pulses the channel A reset lines on all downstream MCIO connectors.

Note:

- Channel a uses PERST# signals on **MCIO pins B11/B12**
- Channel b uses PERST# on **MCIO pins B29/B30**

Port Link Status— showport

The **showport** command displays the link status for all upstream (USP) and downstream (DSP) ports on the Atlas3 PCIe switch. The output shows each port's station number, connector or upstream-port identifier, physical port number, negotiated link speed and width, desired link speed and width, and current link status.



Output Field Descriptions

Field	Description
Station Number	Physical station index on the Atlas3 switch.
Connector / Port ID	Identifies the downstream MCIO connector or upstream PCIe interface associated with the port.
Physical Port Number	Physical switch port number assigned to the interface.
Speed	The **negotiated PCIe generation** (e.g., Gen1, Gen4, Gen6).
Width	The **negotiated link width** (e.g., x1, x4, x8, x16).
Max	The **desired PCIe link** speed and width for the port.
Status	Current link condition (Active, Idle, or Degraded).

Status Definitions

- **Degraded** – Link trained successfully but negotiated speed or width is lower than expected.
- **Idle** – No physical link detected or device not present on the port.
- **Active** – Desired and negotiated link speed/width matched successfully.

Built-In Self-Test — bist

The **bist** command runs a basic diagnostic routine on the Atlas3 32-A0 Host Adapter Card. It checks communication with onboard I²C devices and reports the status of each detected component.

The diagnostic checks communications with onboard I²C devices such as EEPROM, I/O expanders, an I²C multiplexer, clock generators, and clock buffers.

The test runs automatically once invoked and reports **OK** or **FAIL** results for each test item. The following table shows an example of the output:

Channel	Device	Address	Status
CH0	PCA9575-0	0x40	OK
CH0	PCA9575-1	0x42	OK
CH0	PCA9575-2	0x44	OK
CH0	MP2971	0xBE	Fail
CH0	AT24C16	0xA0	OK
CH0	TMP112	0x92	OK
CH3	PCA9548	0xE2	OK
CH1	RC21012	0x12	OK
CH1	RC19016	0xD8	OK

Host Card Mode Configuration — setmode

On hardware revision 1.1 or later, **setmode** selects a preloaded SBR profile for the PCIe Gen 6 host interface and downstream MCIO bifurcation.

Enter **setmode** followed by a mode number from 1 to 8. Each mode determines the Gen 6 precoding setting and downstream MCIO lane configuration. All modes use a common clock:

Mode	Gen6 Precoding	MCIO Bifurcation
1	Enabled	1 x **x16**
2	Enabled	2 x **x8**
3	Enabled	4 x **x4**
4	Enabled	8 x **x2**
5	Disabled	1 x **x16**
6	Disabled	2 x **x8**
7	Disabled	4 x **x4**
8	Disabled	8 x **x2**

Show Host Card Mode — showmode

The **showmode** command displays the currently selected host-card configuration. Use it to check the active SBR mode, including MCIO bifurcation and precoding settings.

PCIe Clock Spread Setting — spread

The **spread** command configures spread-spectrum behavior for the Atlas3 PCIe reference clock. It can operate with spread disabled or with down-spreading of 3,000 ppm or 5,000 ppm.

Enter the command **spread** followed by the **1**, **2**, or **off**:

Command	Clock Behavior
spread 1	3,000 ppm down-spread (-0.3%)
spread 2	5,000 ppm down-spread (-0.5%)
spread off	Spread spectrum disabled

PCIe Clock Output Control – clk

The **clk** command enables or disables the PCIe reference clock outputs at **CN5** and **CN6**. The switch's own reference clock remains enabled.

The setting can be changed during operation and is saved by the MCU for subsequent power cycles.

- **clk en** – Enables reference clock outputs at the external MCIO connectors.
- **clk dis** – Disables reference clock outputs at the external MCIO connectors.

Clock Output Guidelines

- Clock output can be changed dynamically and does not require a host card power cycle.
- The setting is stored in the MCU and applied automatically the next time the host card powers on.
- The Atlas3 switch system reference clock remains enabled regardless of the downstream clock-output setting.

SDB Port Control — sdb

The **sdb** command enables or disables the Atlas3 Serial Debug Bridge (SDB) interface. It determines whether the board remains in normal MCU-controlled CLI operation or makes the SDB interface available for external Broadcom debug utilities.

Enter the command **sdb** followed by **off** or **on**:

Command	Description	Typical Use
sdb off	Sets the MCU SDB state to OFF.	Used for **normal operation** like running CLI commands such as **fdl**, **mw**, **dr**, **dp**, and **showport**.
sdb on	Sets the MCU SDB state to ON.	Used for **utility mode** – running host-based tools such as **SwitchCLID** or **ARCTIC** from a PC.

SDB Behavior Notes

- Only one mode is active at a time (normal MCU/CLI operation or SDB utility access).
- Setting **sdb on** switches the board from normal MCU/CLI operation to SDB access for host-based utilities.

Utilities such as SwitchCLID and ARCTIC are Broadcom-provided tools distributed under NDA and SLA. Contact Broadcom for licensing, access, or additional support information.

UART Path Selection — uart

The **uart** command selects the UART path exposed through USB Type-C connector **CN2**, switching between Atlas3 SDB (Serial Debug) and SMART UART.

Enter the command **uart** followed by **0** or **1**:

- **uart 0** – Routes CN2 to SMART UART
- **uart 1** – Routes CN2 to SDB (default)

UART Path Notes

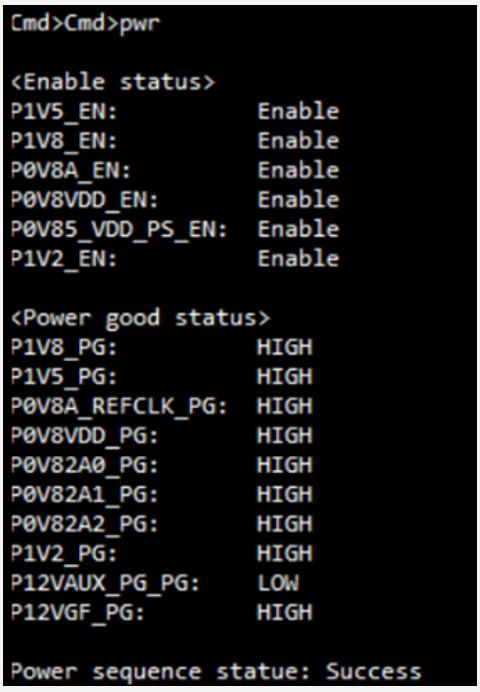
- The selected UART path is stored and applied after a power cycle.
- SDB (Serial Debug) is supported in both managed and unmanaged firmware modes.
- SMART UART is supported only in managed firmware mode.

Power Status — pwr

The **pwr** command displays the current power status of the Atlas3 32-A0 Host Adapter Card, including power-rail enable states, power-good signals, and overall power sequencing status. A “Success” power sequence status indicates all required rails initialized correctly.

The output is organized into:

- **Enable Status** — Shows whether each monitored power rail is enabled or disabled.
- **Power Good Status** — Reports the power-good state for each monitored rail.
- **Power Sequence Status** — Reports whether the board power-up sequence completed successfully.



Port Error Counters — counters

The **counters** command displays error counters for each active port on the Atlas3 PCIe switch. The output includes **PortRx**, **BadTLP**, **BadDLLP**, **RecDiag**, **LinkDown**, and **FlitError** counters, providing a quick view of link and protocol-level errors across the switch.

- **counters** – Displays the current error counts for all ports.
- **counters clear** – Clears the error counters for all ports.

About Error Counter Behavior

- The FLIT error counter increments by 1 when enabled and a countable event occurs, as defined by the FLIT Error Counter Control Register.
- If non-zero, the counter decrements at a fixed rate based on the link encoding and width.
- The counter is cleared when the FLIT Error Counter Enable bit transitions from **0b** to **1b**.

FLIT Mode Control — flit

The **flit** command controls FLIT disable mode on Atlas3 PCIe ports. The setting determines whether a port advertises FLIT mode support during PCIe link training.

Enter **flit** followed by all or station 0 or 2, then **on** or **off**. The command controls the FLIT-disable setting (so on disables FLIT support, while off permits FLIT advertisement). For example:

- **flit 2 off** – Clears FLIT-disable mode for station 2, permitting FLIT support to be advertised.
- **flit all on** – Enables FLIT-disable mode for all stations, preventing FLIT support from being advertised during link training.

About FLIT Disable Mode

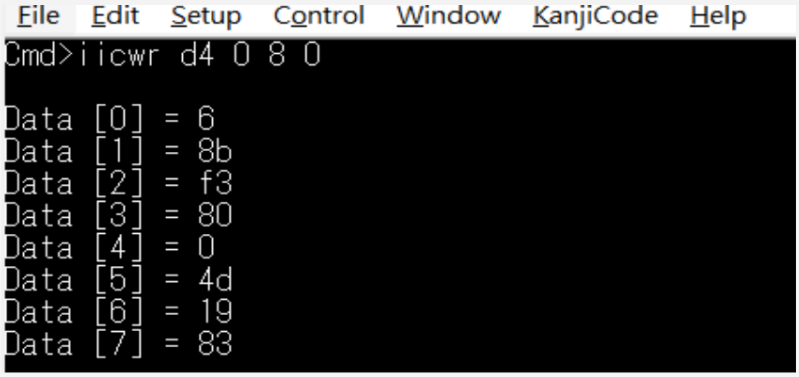
- Enabling FLIT disable mode prevents the port from advertising FLIT support during link training.
- This setting does not modify the FLIT capability reported in PCIe configuration registers.
- FLIT mode is required for operation at 64 GT/s (Gen6). Disabling FLIT will prevent links from training at Gen6 speeds.

SMBus Read — iicwr

The **iicwr** command reads SMBus data from devices connected through the MCIO interfaces. It can be used to access device registers for diagnostics or validation.

Enter **iicwr** followed by the device address (hex), connector number (0–3), number of bytes to read (up to 128), and write-data bytes (hex). For example:

- **iicwr d4 0 8 0** – Reads 8 bytes from SMBus device address 0xD4, starting at register 0x00 on connector 0.



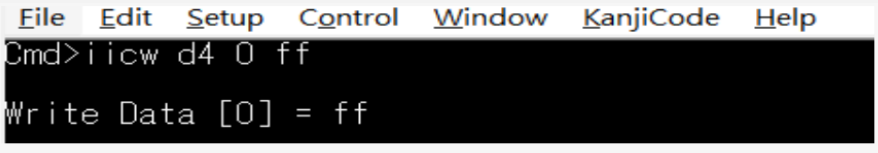
- Channel A uses the I²C interface on MCIO pins B8/B9.
- Channel B uses the I²C interface on MCIO pins B26/B27.

SMBus Write — iicw

The **iicw** command writes SMBus data to devices connected through the MCIO interfaces. It is typically used to write register values or configuration data to attached devices.

Enter **iicw** followed by the device address (hex), connector number (0–3), and one or more hexadecimal data bytes (up to 128 bytes). For example:

- **iicw d4 0 ff** – Writes 0xFF to the device at SMBus address 0xD4 through connector 0.



Bifurcation Mode Programming — bifmode

The **bifmode** command changes the downstream PCIe bifurcation mode by programming a Serial Boot Record (SBR) configuration from the MCU QSPI flash to the Atlas3 switch flash.

Before using this command, run **fdl config** to load the multi-configuration SBR bundle into MCU flash. This bundle contains the predefined bifurcation configurations that bifmode can select.

Enter **bifmode** followed by a mode number (1–8) corresponding to the configurations described under setmode. For example:

- **bifmode 2** — Selects the configuration for two x8 downstream links with Gen 6 precoding enabled.

Link Training Status — ltssm

The **ltssm** command displays the current PCIe Link Training and Status State Machine (LTSSM) state for a selected port. It also supports continuous monitoring during link initialization and troubleshooting.

Enter **ltssm** followed by a port number, optionally using **-p**. For continuous monitoring, specify the sampling interval in milliseconds and the number of readings. Use **ltssm decode** to display the supported LTSSM states and their meanings. For example:

- **ltssm -p 0** — Displays the state of port 0.
- **ltssm 32** — Displays the state of the host-side port.
- **ltssm 32 10 100** — Samples port 32 at 10 ms intervals for 100 readings.
- **ltssm decode** — Displays state decoding.

```
Cmd>ltssm -p 0

Port 0: Counter 0,  State - L0.Active  (301)
Port 0: Counter 1,  State - L0.Active  (301)
Port 0: Counter 2,  State - L0.Active  (301)
Port 0: Counter 3,  State - L0.Active  (301)
Port 0: Counter 4,  State - L0.Active  (301)
Port 0: Counter 5,  State - L0.Active  (301)
Port 0: Counter 6,  State - L0.Active  (301)
Port 0: Counter 7,  State - L0.Active  (301)
Port 0: Counter 8,  State - L0.Active  (301)
Port 0: Counter 9,  State - L0.Active  (301)
Port 0: Counter 10, State - L0.Active  (301)
Port 0: Counter 11, State - L0.Active  (301)
Port 0: Counter 12, State - L0.Active  (301)
Port 0: Counter 13, State - L0.Active  (301)
Port 0: Counter 14, State - L0.Active  (301)
Port 0: Counter 15, State - L0.Active  (301)
Cmd>
```

```
Cmd>ltssm 32

Port 32: Counter 0,  State - L0.Active  (301)
Port 32: Counter 1,  State - L0.Active  (301)
Port 32: Counter 2,  State - L0.Active  (301)
Port 32: Counter 3,  State - L0.Active  (301)
Port 32: Counter 4,  State - L0.Active  (301)
Port 32: Counter 5,  State - L0.Active  (301)
Port 32: Counter 6,  State - L0.Active  (301)
Port 32: Counter 7,  State - L0.Active  (301)
Port 32: Counter 8,  State - L0.Active  (301)
Port 32: Counter 9,  State - L0.Active  (301)
Port 32: Counter 10, State - L0.Active  (301)
Port 32: Counter 11, State - L0.Active  (301)
Port 32: Counter 12, State - L0.Active  (301)
Port 32: Counter 13, State - L0.Active  (301)
Port 32: Counter 14, State - L0.Active  (301)
Port 32: Counter 15, State - L0.Active  (301)
```

```
Cmd>ltssm decode

--- Broadcom Atlas3 LTSSM Decode Table ---
 Code   State Name
 ----------------------------
 0x000  Detect.Quiet
 0x001  Detect.Active
 0x002  Detect.Rate
 0x003  Detect.Wait12ms
 0x004  Detect.P1_Req
 0x005  Detect.Donest
 0x006  Detect.P0_Req
 0x007  Detect.RateOk
 0x009  Detect.SpcOp
 0x101  Polling.P0_Req
 0x103  Polling.Active
 0x106  Polling.Done
 0x107  Polling.Cfg
 0x10A  Polling.TxEIOS
 0x10B  Polling.Compliance
 0x10E  Polling.EIdle
 0x10F  Polling.Speed
 0x200  Cfg.Idle
 0x201  Cfg.Lw_Start_Dn
 0x202  Cfg.Ln_Wait_Dn
 0x203  Cfg.Lw_Accept_Dn
 0x204  Cfg.TxIdle
 0x206  Cfg.Ln_Accept_Dn
 0x207  Cfg.Complete_Dn
 0x208  Cfg.Ln_Wait_Up
 0x20C  Cfg.Ln_Accept_Up
 0x20E  Cfg.Done_St
 0x20F  Cfg.TxCtlSkip
 0x210  Cfg.Lw_Start_Up
 0x211  Cfg.XLinkArb_Won
 0x214  Cfg.TxSDSM
 0x218  Cfg.Lw_Accept_Up
 0x21C  Cfg.Complete_Up
 0x300  L0.Idle
 0x300  L0.Idle
 0x301  L0.Active
 0x302  L0.L0s
 0x303  L0.TxEIOS
 0x304  L0.LinkDown
 0x305  L0.LDWait
 0x307  L0.L1
 0x309  L0.Recovery
 0x30D  L0.ActRec
 0x400  Recovery.Idle
 0x401  Recovery.RcvrLock
 0x402  Recovery.TxEIOS
 0x403  Recovery.RcvrCfg
 0x405  Recovery.EqPhase1_Dn
 0x407  Recovery.Speed
 0x408  Recovery.TxEIEOS
 0x409  Recovery.HotReset
 0x40A  Recovery.Disable
 0x40B  Recovery.TxIdle
 0x40C  Recovery.ErrCfg
 0x40D  Recovery.TxSDSM
 0x40E  Recovery.ErrDet
 0x40F  Recovery.Loopback
 0x410  Recovery.EqPhase3_Up
 0x411  Recovery.EqPhase0_Up
 0x415  Recovery.EqPhase2_Dn
 0x417  Recovery.EqPhase3_Dn
 0x418  Recovery.EqPhase2_Up
 0x419  Recovery.EqPhase1_Up
 0x41E  Recovery.TxCtlSkip
 0x41F  Recovery.MyEqPhase
 0x500  Loopback.Idle
 0x501  Loopback.Entry
 0x506  Loopback.TxEIOS
 0x509  Loopback.ActMaster
 0x50A  Loopback.ActSlave
 0x50B  Loopback.ExitSt
 0x50C  Loopback.Speed
 0x50F  Loopback.EIdle
 0x600  HotReset.Idle
 0x601  HotReset.Dir
 0x602  HotReset.Rcvr
 0x603  HotReset.Tx
 0x604  HotReset.TxEIOS_1
 0x605  HotReset.TxEIEOS
 0x606  HotReset.RcvWait
 0x607  HotReset.TxEIOS
 0x800  LowPower.Idle
 0x801  L0s.Entry
 0x802  L0s.Idle
 0x803  L0s.TxFTS
 0x804  L0s.TxSKP
 0x80A  L0s.TxEIE
 0x80C  L0s.TxSDSM
 0x900  LowPower.Idle
 0x905  L1.RxEIOS
 0x906  L1.Idle
 0xA00  LowPower.Idle
 0xA08  L2.RxEIOS
 0xA09  L2.Rate
 0xA0D  L2.RateOk
 0xA0F  L2.Idle
```

PCIe FLIT Diagnostics — flitdiag

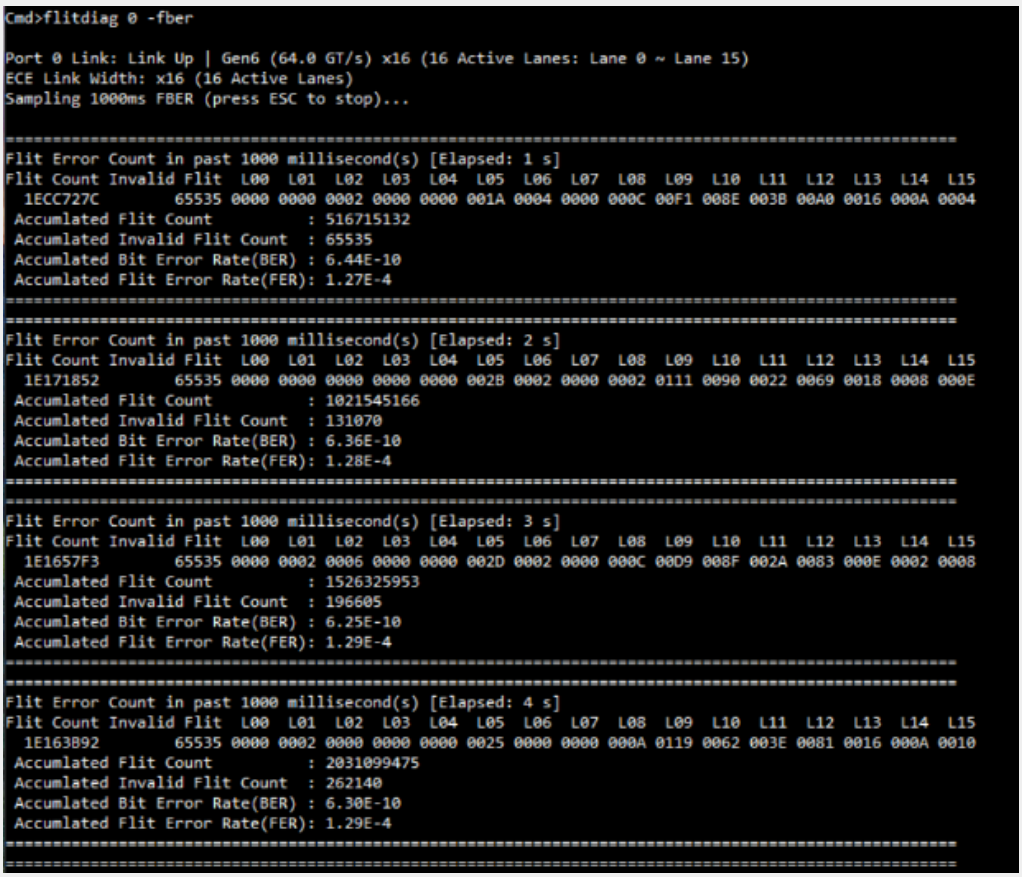
The **flitdiag** command displays PCIe Gen 6 FLIT-level diagnostics for a selected port, including FLIT bit errors, lane bit errors, and error-counter information. It also supports clearing diagnostic counters.

Enter **flitdiag** followed by a port number and an optional diagnostic parameter. The available parameters are listed below:

Parameter	Description
-fber	Displays FLIT bit-error information
-lnber	Displays lane-bit error information
-errcnt [0-3]	Selects an error counter (0-3)
clear	Clears diagnostic counters

For example:

- **flitdiag 0** — Displays FLIT diagnostics for port 0.
- **flitdiag 0 -fber** — Displays FLIT bit-error information.
- **flitdiag 0 -lnber** — Displays lane bit-error information.
- **flitdiag 0 -errcnt 2** — Selects error counter 2.
- **flitdiag clear** — Clears FLIT diagnostic counters.



PCIe Link Speed Control — speed

The **speed** command displays the current PCIe target link speed or sets a target generation and initiates link retraining. It supports individual PCIe ports and station identifiers.

Enter **speed** without parameters to display the current speed setting. To change the target speed, enter a port number followed by the desired PCIe generation (1–6). Alternatively, use **stn** followed by a station number (0 or 2) and the target generation. For example:

- **speed** – Displays the current speed setting.
- **speed 0 5** – Sets port 0 to Gen 5 and retrains the link.
- **speed 32 6** – Sets host-side port 32 to Gen 6 and retrains the link.
- **speed stn 0 gen4** – Sets station 0 to Gen 4.

Link training depends on the capabilities of both connected endpoints.

```
Cmd>speed

--- PCIe Link Speed & Capability Overview ---
Port  Max Capable    Target Speed    Current Link   Status
-------------------------------------------------------------
0     Gen6           Gen6            Gen6 x16       Link Up
32    Gen6           Gen6            Gen6 x16       Link Up
-------------------------------------------------------------
Usage to set speed:
  speed <port> <1~6>           : Set target speed on specific port
  speed stn <0|2> <1~6>        : Set target speed on entire station
  (Station 0: Port 0~15, Station 2: Port 32~47)
Cmd>
```

MCTP Command – mctp

The **mctp** command sends Management Component Transport Protocol (MCTP) commands to connected devices. It supports device identification, health monitoring, and management operations through the selected slot.

Enter **mctp** followed by a slot number (0–3) and one of **sn**, **health**, **pause**, **resume**, **abort**, **status**, or **replay**. For example:

- **mctp 1 sn** – Requests the serial number of the device in slot 1
- **mctp 1 health** – Requests health status information from the device in slot 1

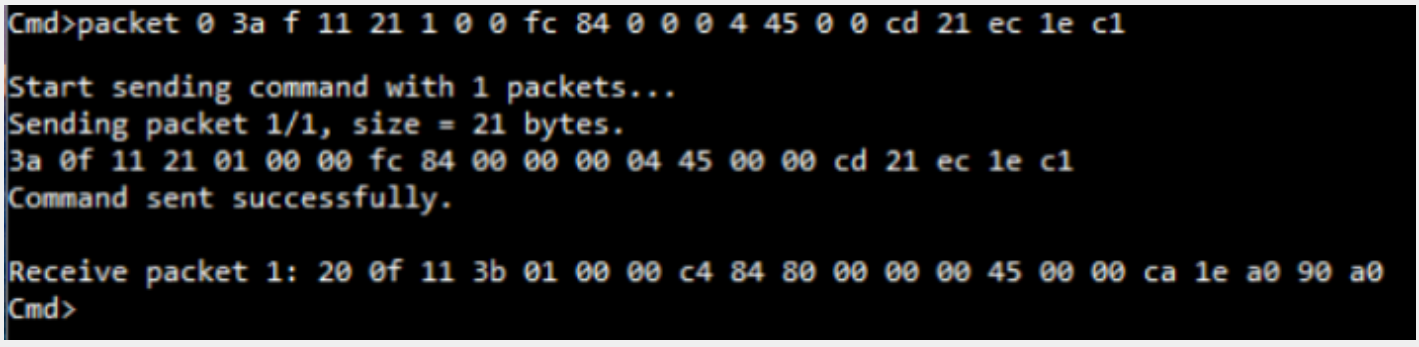


MCTP Packet – packet

The **packet** command sends raw Management Component Transport Protocol (MCTP) packet data to a device in the selected slot. It allows users to transmit hexadecimal packet data for device communication and debugging.

Enter packet followed by a slot number (0–3) and up to 128 bytes of hexadecimal packet data. For example:

- **packet 0 3a f 11 21 1 0 0 fc 84 0 0 0 4 45 0 0 cd 21 ec 1e c1** – Sends the specified hexadecimal packet data to slot 0



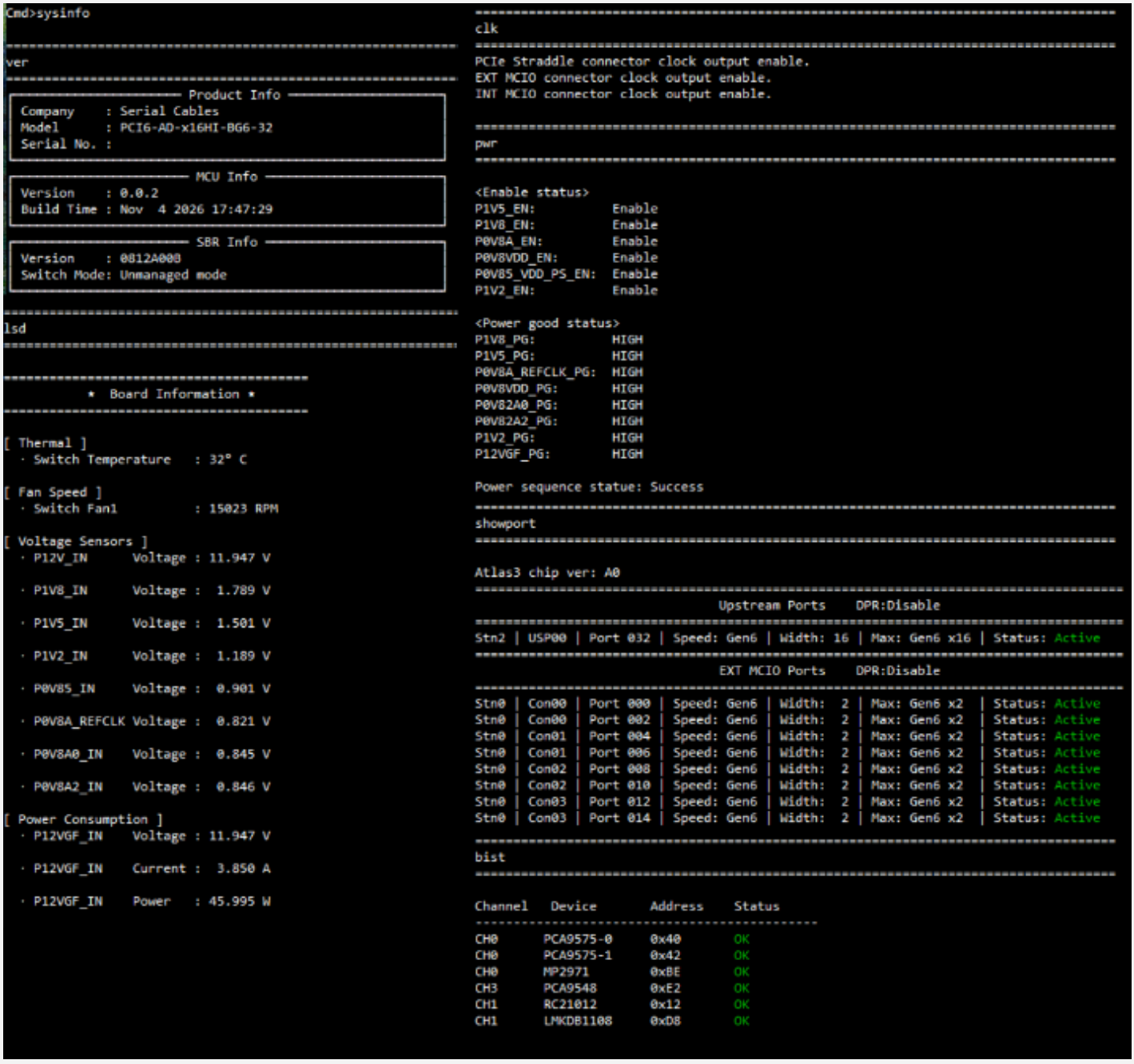
System Version — ver

The **ver** command displays host card identification and version information for the MCU and Atlas3 switch. Use it to verify the running firmware and switch mode before or after a firmware update.

System Information — sysinfo

The **sysinfo** command displays a complete summary of the Atlas3 32-A0 Host Adapter Card's configuration and operating status, including firmware information, board telemetry, power status, PCIe link state, clock configuration, and onboard device diagnostics.

This is effectively a sequence of several key commands consolidated into a single report for quick system validation.



System Reset — reset

The **reset** command supports an MCU reset, a switch system power-on reset, and resets for the available PCIe hierarchy signals.

Enter **reset** without parameters to reset the onboard MCU, or specify a reset type (**sw**, **s0**, or **s1**) to perform a different reset operation. For example:

- **reset** – Reset the onboard MCU
- **reset s0** – Pulses the S0 PCIe hierarchy reset signal.
- **reset sw** – Triggers the Atlas3 switch system power-on reset (**SYS_PWR_ON_RST_N**).
- **reset s1** – Pulses the S1 PCIe hierarchy reset signal.

The **reset** command can also be used after an MCU firmware update to activate the new firmware without power cycling the host card.

Maintenance and Diagnostics

The Atlas3 32-A0 Host Adapter Card includes CLI commands and onboard indicators for monitoring system health and PCIe connectivity. The following checks can help identify common issues during installation, testing, or troubleshooting.

- **For a general system check**, run **sysinfo** to collect firmware information, board telemetry, power status, PCIe link state, clock configuration, and onboard device diagnostics in a single report.

- **If a PCIe link does not train as expected**, run **showport** to compare the negotiated and desired link speed and width. A **Degraded** status indicates that the negotiated speed or width does not match the desired configuration. Use **counters** to check for accumulated port errors.

- **If a power issue is suspected**, run **pwr** to check power-rail enable states, power-good signals, and sequencing status. Use **lsd** to review voltage readings and power consumption.

- **If the Atlas3 System Error LED (LED2) is illuminated**, run **bist** to check communication with onboard I²C devices and **lsd** to review temperature, voltage, fan speed, and power telemetry.

- After a firmware update, use **ver** to check the firmware version. Power-cycle the card after switch firmware updates; apply MCU firmware with reset.

Revision History

Revision	Description
1.1	Reformatted and restyled for brand consistency and readability. Rewritten for clarity. Added *Product Overview, Safety, Handling & Compliance, Maintenance & Diagnostics,* and *Contact Us* sections.
1.0	Initial manual release.

Contact Us

For technical assistance, product inquiries, or additional documentation, our team is here to help.

Support

📧 **support@serialcables.com**

Sales

📧 **sales@serialcables.com**

Phone

📞 **+1 (303) 495-2320**

Website

🌐 **https://serialcables.com/**