PCIe 6.0 / CXL x16 dual E3, 2T Adapter

TECHNICAL MANUAL



Revision 1.1 Sep 2026

PCI6-AD-x162x8-EDSFF

PCI EXPRESS 6.0

CXL Compute Express Link™

SSD

Fits any E3, 2T NVMe SSD

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Declaration and Revision Notice

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Product Overview

The Serial Cables PCI6-AD-x162x8-EDSFF is a PCIe adapter card that connects to a host through a PCIe x16 edge connector and provides two x8, 84-pin right-angle EDSFF device connectors. The board also provides dedicated headers for EDSFF power-disable control, MFG and FRU signals, reset access, HLED control, dual-port selection, and SMBus access.

EDSFF device power can be sourced from the host PCIe interface or from the onboard PCIe 2x6 auxiliary power connector. SW1 selects between these power paths. Two onboard fan connectors support the cooling assemblies shown in the supplied hardware configuration.



Key Features

- **Dual x8 EDSFF Interfaces –** Two 84-pin right-angle EDSFF connectors provide the device interfaces.
- **PCIe x16 Host Connection –** The board connects to the host through its PCIe edge connector (golden finger).
- **Selectable EDSFF Power Source –** SW1 selects host-provided power or the PCIe 2x6 auxiliary power input.
- **Per-Device Control Headers –** Header pairs provide access to PWRDIS, reset, HLED, and dual-port control functions for the EDSFF interfaces.
- **SMBus Access –** J1 and J2 can bridge the host SMBus to the EDSFF device or expose EDSFF SMBus lines to an external I²C analyzer.

Safety, Handling, and Compliance

The PCI6-AD-x162x8-EDSFF should be installed and handled using standard PCIe hardware and ESD-safe procedures. Follow the precautions below when installing, configuring, or servicing the adapter.

Electrical Safety

Follow these precautions when installing, configuring, or servicing the adapter:

- Power down the host system before installing or removing the adapter or EDSFF devices. Disconnect system power before changing the auxiliary power connection.
- Set **SW1** to the intended power source before applying power to the host system.
- If **SW1** is set to the auxiliary-power position, confirm that **CN3** is connected to the intended PCIe 2x6 power source before startup.

ESD Protection

The adapter contains components that can be damaged by electrostatic discharge.

- Work only in an electrostatic discharge-safe area with a grounded mat and wrist strap.
- Keep the card in its anti-static packaging until you are ready to install it.
- Avoid touching connector pins, exposed traces, or any metallic contacts.

Thermal and Airflow Considerations

The adapter provides J13 and J14 fan connections for cooling the installed EDSFF devices.

- Maintain clear airflow around the adapter.
- Do not obstruct either fan or the EDSFF device area beneath it.

Compliance

This product is manufactured in accordance with standard international safety and environmental regulations.

Hardware Specifications

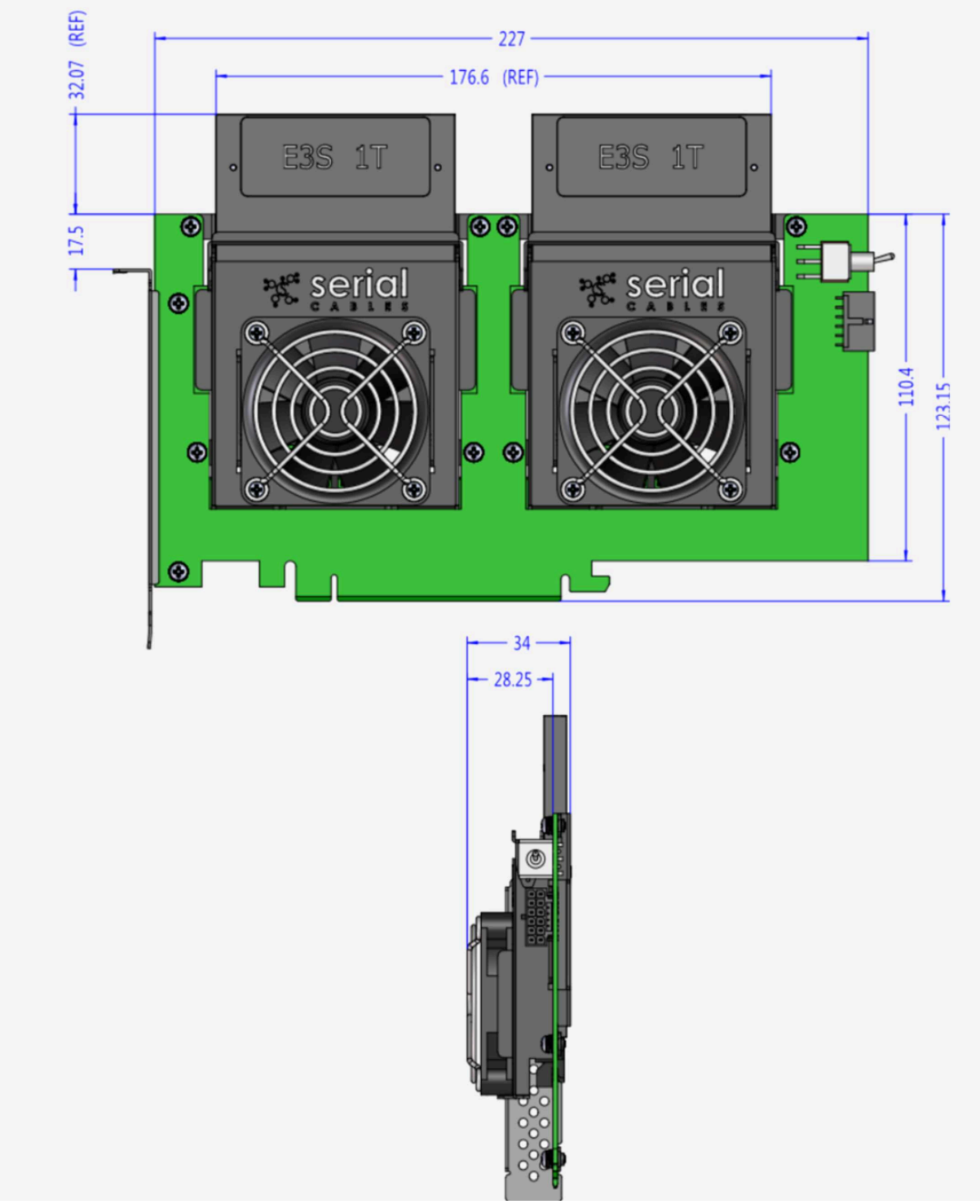
Parameter	Specification
Product	PCI6-AD-x162x8-EDSFF
Host Interface	PCIe x16 edge connector (golden finger)
EDSFF Interfaces	2 x x8, 84-pin right-angle EDSFF connectors (CN1 and CN2)
EDSFF Power Sources	Host PCIe interface or CN3 auxiliary power input
Power Selection	SW1 toggle switch selects the EDSFF power source
Auxiliary Power Connector	CN3, PCIe 2x6 power connector
Fan Connectors	J13 and J14, 2.54 mm-pitch fan connectors
Internal Headers	J1–J12 provide SMBus access, PWRDIS control, MFG/FRU signal access, reset, HLED control, and dual-port configuration
Mechanical Envelope	227 mm overall width × 123.15 mm overall height; 34 mm depth at the location shown in the mechanical drawing

Power Requirements

The adapter provides two selectable power paths for the attached EDSFF devices. SW1 determines which source feeds the EDSFF power path. The host PCIe edge connector is the host-power source and CN3 is the auxiliary PCIe 2x6 power source.

Adapter Card Dimensions

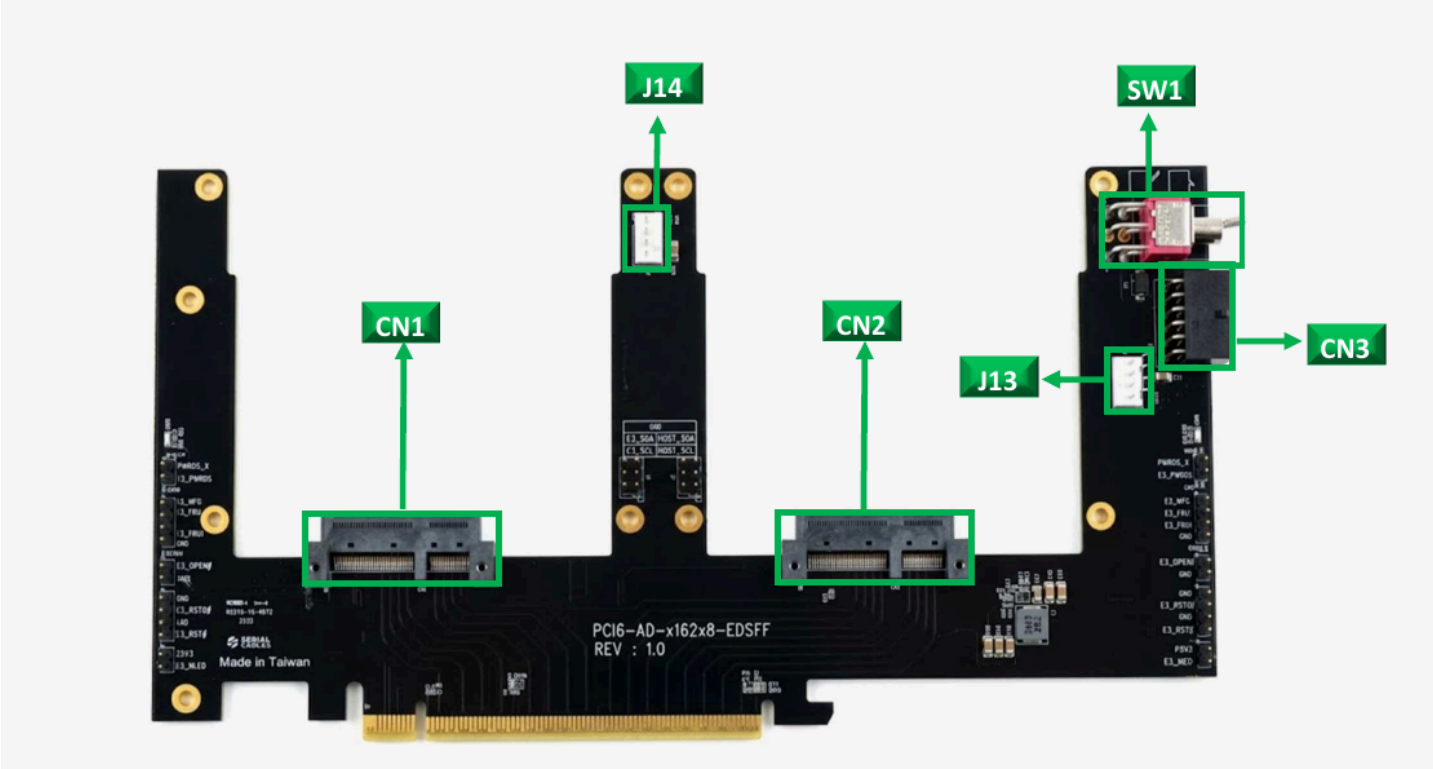
The mechanical drawing below shows the adapter with two EDSFF devices and cooling assemblies installed. Dimensions are shown in millimeters. Dimensions marked REF are reference dimensions.



Connector Locations and Functions

The adapter's main device and power connections, along with the fan headers and SW1 power-selection switch, are identified below. The designators shown in the figure correspond to the markings silk-screened on the PCB and are used throughout this manual.

Designator	Connector Type	Function / Description
CN1	x8 84-pin right-angle EDSFF connector	Provides one x8 EDSFF device interface.
CN2	x8 84-pin right-angle EDSFF connector	Provides the second x8 EDSFF device interface.
CN3	PCIe 2x6 power connector	Provides the auxiliary power source used when SW1 is set to the DOWN position.
SW1	Toggle switch	Selects EDSFF device power from the host PCIe edge connector or CN3.
J13 / J14	2.54 mm-pitch fan connectors	Provide connections for two board-mounted cooling fans.



CN1 / CN2 – EDSFF x8 Connectors

CN1 and CN2 are **84-pin, right-angle EDSFF connectors**, each providing an x8 device interface. Both connectors use the same interface type and are located above the PCIe x16 edge connector in the board layout.

Additional device control and monitoring functions are available through the onboard header pairs described later in this manual. These headers provide access to PWRDIS, MFG/FRU signals, PERST#, HLED, dual-port configuration, and SMBus connectivity for the corresponding EDSFF interfaces.

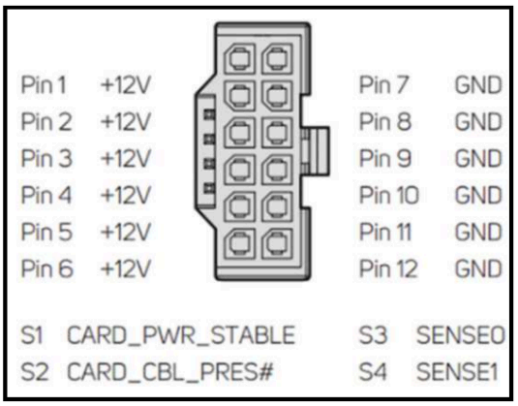
CN3 – PCIe 2x6 Power Connector

CN3 provides the auxiliary power input for the EDSFF device power path. When SW1 is in the DOWN position, the EDSFF devices are powered through CN3 instead of through the host PCIe golden finger.

The connector includes 12 primary power contacts, consisting of six +12 V contacts and six ground contacts, along with four sideband contacts:

Pin	Signal
1 - 6	+12 V
7 - 12	GND

Sideband	Signal
S1	CARD_PWR_STABLE
S2	CARD_CBL_PRES#
S3	SENSE0
S4	SENSE1



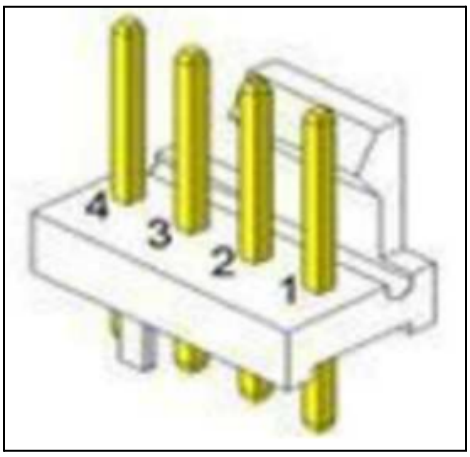
SW1 – EDSFF Power Source Selection

SW1 selects the power source for the attached EDSFF devices. In the UP position, device power is supplied through the host PCIe edge connector. In the DOWN position, power is supplied through CN3, the auxiliary PCIe 2x6 power connector.

SW1 Position	EDSFF Power Source	Selected Source
UP	Host PCIe interface (golden finger)	Host / PCIe golden finger
DOWN	CN3 PCIe 2x6 power connector	CN3 / PCIe 2x6 auxiliary power connector

J13 / J14 – Fan Connectors

J13 and J14 are 2.54 mm-pitch fan connectors that provide the connection points for the two fan assemblies mounted over the installed EDSFF devices. Each header serves one of the cooling assemblies shown in the board layout.



Internal Headers

The PCI6-AD-x162x8-EDSFF uses paired headers to provide control, status, and management access for each EDSFF interface. J1 through J12 are identified in the layout below, with corresponding header pairs serving the same function for each device interface.

Headers	Function
J1 / J2	EDSFF SMBus access and host-SMBus bridging
J3 / J4	PWRDIS configuration
J5 / J6	MFG and FRU signal-level access
J7 / J8	EDSFF PERST# manual reset access
J9 / J10	HLED control
J11 / J12	Dual-port enable / disable



J1 / J2 – SMBus Access Headers

J1 and J2 provide SMBus access for the two EDSFF interfaces. Each header can connect the EDSFF SMBus clock and data signals to the host SMBus on the PCIe golden finger, or provide direct access to the EDSFF SMBus for an external I²C analyzer.

To connect the EDSFF SMBus to the host, install jumpers across **pins 1–2** and **pins 3–4**. This connects **HOST_SMCLK** to **EDSFF_SMCLK** and **HOST_SMDAT** to **EDSFF_SMDAT**.

For external I²C analyzer access, use **pin 2** for **EDSFF_SMCLK**, **pin 4** for **EDSFF_SMDAT**, and **pin 6** for ground.

Header Pin	Signal	Associated Interface Pin
1	HOST_SMCLK	GF_B5
2	EDSFF_SMCLK	EDSFF_A7
3	HOST_SMDAT	GF_B6
4	EDSFF_SMDAT	EDSFF_A8
5	GND	–
6	GND	–

J3 / J4 – PWRDIS Headers

J3 and J4 control the PWRDIS signal for the corresponding EDSFF interface. The jumper state determines whether device power is enabled or disabled.

Jumper Configuration

When the jumper is installed, the 3.3 V, 1 kΩ pull-up sets **EDSFF_PWRDIS** **HIGH**. With the jumper removed, **EDSFF_PWRDIS** is **LOW**.

Jumper State	PWRDIS State	Device Power
ON	HIGH (H)	EDSFF power disable
OFF	LOW (L)	EDSFF power enable

Header Pinout

Header Pin	Signal	Associated EDSFF Pin
1	P3V3 Pull 1K	–
2	EDSFF_PWRDIS	EDSFF_B12

J5 / J6 – MFG and FRU Headers

J5 and J6 provide access to the **MFG and FRU sideband signals** for each EDSFF interface. The headers allow the signal levels to be checked directly at the board.

Header Pin	Signal	Associated EDSFF Pin
1	EDSFF_MFG	EDSFF_B7
2	EDSFF_FRU	EDSFF_B8
3	EDSFF_FRU1	EDSFF_A42
4	GND	–

J7 / J8 – PERST# Reset Headers

J7 and J8 provide manual access to the reset signals for the corresponding EDSFF interface. **EDSFF_PERST0#** is the primary PCIe reset signal, used to place the connected EDSFF device in reset so the PCIe interface can be reinitialized. The signal is available on header pin 2 and maps to EDSFF pin B10.

Header Pin	Signal	Associated EDSFF Pin
1	GND	–
2	EDSFF_PERST0#	EDSFF_B10
3	GND	–
4	EDSFF_P11	EDSFF_A11

J9 / J10 – HLED Headers

J9 and J10 provide access to the **HLED control signal** for the corresponding EDSFF interface. Each two-pin header provides the control point for the HLED signal associated with that device.

Header Pin	Signal	Associated EDSFF Pin
1	PCIE_P3V3	–
2	EDSFF_HLED	EDSFF_A10

J11 / J12 – Dual-Port Enable Headers

J11 and J12 configure the corresponding EDSFF interface for single-port or dual-port operation.

Jumper Configuration

Installing the jumper connects **EDSFF_DPEN#** to ground and selects dual-port operation. Removing the jumper selects single-port operation.

Jumper State	Interface Mode
ON	Dual-port
OFF	Single-port

Header Pinout

Header Pin	Signal
1	EDSFF_DPEN#
2	GND

Configuration and Bring-Up Checklist

Before applying power, verify that the adapter is configured for the intended EDSFF setup:

1. Set **J11/J12** for the required single-port or dual-port mode.
2. Check the **J3/J4 PWRDIS** jumper state. Jumper ON sets PWRDIS HIGH and disables EDSFF device power; jumper OFF sets PWRDIS LOW and enables device power.
3. Configure **J1/J2** for either host SMBus connectivity or external I²C analyzer access, as required.
4. Set **SW1** to the intended EDSFF power source. Use the UP position for power from the host PCIe edge connector or the DOWN position for power through CN3.
5. If CN3 power is selected, connect the PCIe 2x6 auxiliary power source before startup.
6. Confirm that the fan assemblies are connected to **J13/J14** before operating the adapter.

Maintenance & Diagnostics

Use the checks below to verify adapter configuration and connections when an EDSFF device does not operate as expected.

- **If an EDSFF device does not power on,** verify the **SW1** power-source setting. If SW1 is in the DOWN position, confirm that **CN3** is connected. Check **J3/J4** and confirm that PWRDIS is not set HIGH.
- **If an EDSFF device does not reset or initialize as expected,** check the **J7/J8** reset connection and confirm the required single-port or dual-port setting at **J11/J12**.
- **If host SMBus access is unavailable,** confirm that **J1/J2** have jumpers installed across pins **1–2** and **3–4**.
- **If an external I²C analyzer cannot access the EDSFF bus,** connect to **J1/J2 pin 2** for **EDSFF_SMCLK**, **pin 4** for **EDSFF_SMDAT**, and **pin 6** for ground.
- **If a cooling fan is not operating,** check the corresponding **J13/J14** connection and confirm that the fan cable is fully seated.

Revision History

Revision	Description
1.1	Reformatted and restyled for brand consistency and readability. Rewritten for clarity. Added *Product Overview*, *Safety, Handling & Compliance*, *Maintenance & Diagnostics,* and *Contact Us* sections.
1.0	Initial manual release.

Contact Us

For technical assistance, product inquiries, or additional documentation, our team is here to help.

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