SERIAL CABLES

PCIe 6.0 MCIO Host Card

Broadcom PEX90064 Atlas III 64-lane Switch Chip

TECHNICAL MANUAL



Revision 1.1 Nov 2026

PCI6-AD-x16HI-BG6-64

Quarch Ready

Command-line interface for monitoring

PCI EXPRESS 6.0

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Declaration and Revision Notice

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Product Overview

The Serial Cables **Atlas3 64-A0 Host Adapter Card** (PCI6-AD-x16HI-BG6-64) is a PCIe Gen 6 adapter built around the **Broadcom PEX90064 Atlas3 switch**. Supporting up to 64 PCIe lanes and 40 ports, the card provides flexible connectivity between a host system and external PCIe devices through four MCIO x8 connectors and a PCIe straddle-mount connector.

The adapter supports both unmanaged operation without managed firmware and managed operation with firmware. An onboard microcontroller provides command-line interface (CLI) functionality for switch configuration, device management, diagnostics, and troubleshooting. Additional capabilities include non-transparent port support, peer-to-peer data transfers, and PCIe hot-plug functionality.



Key Features

- **PCIe Gen 6 performance** – Broadcom PEX90064 switch supporting up to 64 lanes and 40 ports.
- **Flexible connectivity** – Four MCIO x8 connectors and one PCIe straddle-mount connector.
- **Low-latency performance** – Supports PCIe Gen 6 FLIT mode and Forward Error Correction (FEC).
- **Managed and unmanaged operation** – Supports firmware-based management and operation without managed firmware.
- **Advanced PCIe functionality** – Non-transparent ports, peer-to-peer transfers, DMA, and hot-plug support.
- **Integrated management** – Onboard microcontroller with CLI access for configuration, diagnostics, and firmware updates.
- **Power options –** Host PCIe slot power or auxiliary 12V input.

Safety, Handling, and Compliance

The Atlas3 64-A0 Host Adapter Card should be installed and handled using standard PCIe hardware and ESD-safe procedures. Follow the precautions below when installing, configuring, or servicing the card.

Electrical Safety

- Power down the host system and disconnect external power supplies before installing, removing, or changing connections to the card.
- Verify the voltage and connector pinout before connecting an auxiliary 12 V power supply.
- Do not connect or disconnect power cables while the system is energized.
- Inspect cables and connectors for damage before use.

ESD Protection

- Work in an ESD-safe area using a grounded mat and wrist strap.
- Keep the card in antistatic packaging until installation.
- Avoid touching connector contacts, exposed traces, or component leads.

Thermal and Airflow Considerations

- Maintain adequate airflow around the Broadcom PEX90064 switch and surrounding components.
- Keep ventilation paths unobstructed during operation.
- Follow the host system's cooling requirements to prevent excessive operating temperatures.

Compliance

This product should be installed and operated in accordance with applicable electrical safety and electromagnetic compatibility (EMC) requirements.

Hardware Specifications

The Atlas3 64-A0 Host Adapter Card is built around the Broadcom PEX90064 PCIe Gen 6 switch, providing high-speed connectivity across multiple PCIe interfaces.

Parameter	Specification
Part Number	PCI6-AD-x16HI-BG6-64
PCIe Switch	Broadcom Atlas3 PEX90064
PCIe Generation	PCIe Gen 6
PCIe Lanes	Up to 64 lanes
PCIe Ports	Up to 40 ports
Operating Modes	Managed and unmanaged
MCIO Connectors	4 x right-angle MCIO x8 (SFF-TA-1016)
PCIe Interface	PCIe straddle-mount connector
Management Interfaces	2 x USB Type-C connectors for Atlas3 debug/UART and onboard MCU access
Auxiliary Power Connector	PCIe 12 V 2x6 power connector
Maximum Power Consumption	60W (Gen6 x64 links, excluding power supplied to the PCIe straddle-mount connector)
Operating Temperature	0°C to +40°C
PCB Dimensions	209 x 136 x 44 mm (L x H x T), including heatsink

Power Requirements

The Atlas3 64-A0 supports two power configurations, depending on the connected devices and system setup:

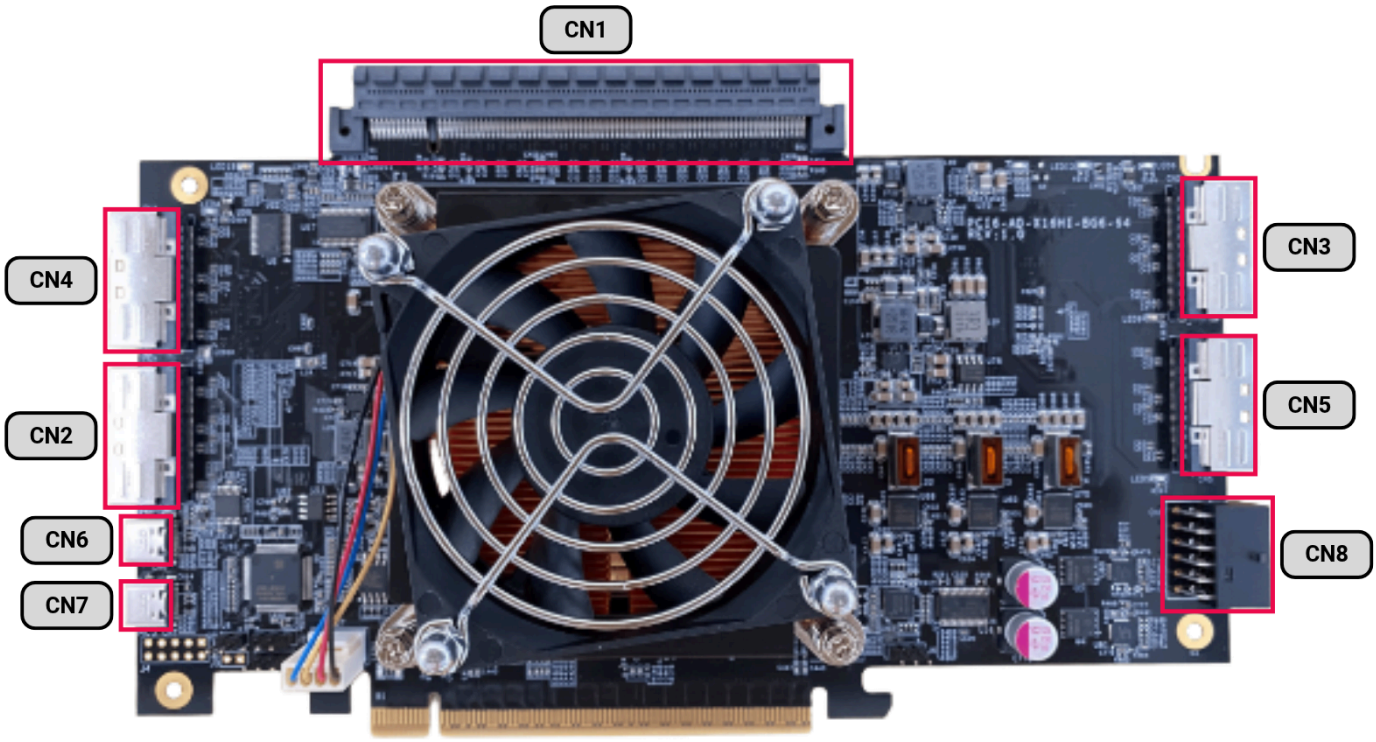
- **Host PCIe Slot Power** – The card can receive power through the host PCIe slot when no device is connected to the PCIe straddle-mount connector.

- **Auxiliary 12 V Power** – The PCIe 12 V 2×6 connector supplies power to the adapter and its cooling assembly, with up to 75 W available to the PCIe straddle-mount connector for a connected device.

Connector Locations and Functions

The following table identifies the connectors on the Atlas3 64-A0 Host Adapter Card, including their functions and associated PCIe lane assignments:

Designator	Connector Type	Function / Description
CN1	PCIe Gen 6 straddle-mount connector	Provides a PCIe connection for a compatible device.
CN2	MCIO x8 (SFF-TA-1016)	Routes PCIe lanes 40-47.
CN3	MCIO x8 (SFF-TA-1016)	Routes PCIe lanes 16-23.
CN4	MCIO x8 (SFF-TA-1016)	Routes PCIe lanes 32-39.
CN5	MCIO x8 (SFF-TA-1016)	Routes PCIe lanes 24-31.
CN6	USB Type-C	Provides access to the Atlas3 I²C slave interface and switchable SDB/Smart UART interface.
CN7	USB Type-C	Provides access to the onboard MCU command-line interface (CLI).
CN8	PCIe 12 V 2x6 auxiliary power connector	Powers the adapter and cooling assembly, supplying up to 75 W to the PCIe straddle-mount connector.



CN1 – PCIe Gen 6 Straddle-Mount Connector

CN1 provides a PCIe Gen 6 connection for compatible devices, with up to 75 W of power available when using auxiliary 12 V power.

CN2 – CN5 – MCIO x8 Connectors

The four MCIO x8 connectors provide PCIe Gen 6 connectivity to external devices. Each connector supports eight PCIe lanes and includes the following sideband signals:

- **Reference Clocks** – Four dedicated PCIe HCSL clock outputs at pins A8/A9, A11/A12, A26/A27, and A29/A30.
- **I²C Interfaces** – Two dedicated interfaces at pins B8/B9 and B26/B27.
- **Reset Signals** – Four PERST# signals at pins B11, B12, B29, and B30.

The following tables detail the PCIe lane and sideband signal assignments for MCIO connector **CN2**. The remaining MCIO connectors use the same pin arrangement, with lane assignments corresponding to their respective interfaces:

	2	3	5	6	8	9
A	PERN40	PERP40	PERP41	PERN41	MCIO_CLKA_P0	MICO_CLKA_N0
B	PETN40	PETP40	PETP41	PETN41	MCIO_SCL_A0	MCIO_SDA_A0
	14	15	17	18	11	12
A	PERN42	PERP42	PERP43	PERN43	MCIO_CLKA_P1	MCIO_CLKA_N1
B	PETN42	PETP42	PETP43	PETN43	MCIO_PERST#_A0	MCIO_PERST#_A1

	20	21	23	24	26	27
A	PERN44	PERP44	PERP45	PERN45	MCIO_CLKB_P0	MICO_CLKB_N0
B	PETN44	PETP44	PETP45	PETN45	MCIO_SCL_A0	MCIO_SDA_A0
	32	33	35	36	29	30
A	PERN46	PERP46	PERP47	PERN47	MCIO_CLKB_P1	MCIO_CLKB_N1
B	PETN46	PETP46	PETP47	PETN47	MCIO_PERST#_B0	MCIO_PERST#_B1

CN6 – CN7 – USB Type-C Connectors

The two USB Type-C connectors provide access to the adapter's management and debug interfaces:

- **CN6** – Atlas3 I²C slave interface and switchable SDB/Smart UART interface.
- **CN7** – Onboard MCU command-line interface (CLI) for configuration, monitoring, and diagnostics.

CN8 – Auxiliary 12 V Power Connector

CN8 is a PCIe 12 V 2×6 auxiliary power connector that supplies power to the Atlas3 64-A0 Host Adapter Card and its cooling assembly. It also provides up to 75 W to the PCIe straddle-mount connector for an installed device.

Pin	Signal
1 - 6	+12V
7 - 12	GND
S1	CARD_CBL_STABLE
S2	CARD_CBL_PRES#
S3	SENSE0
S4	SENSE1

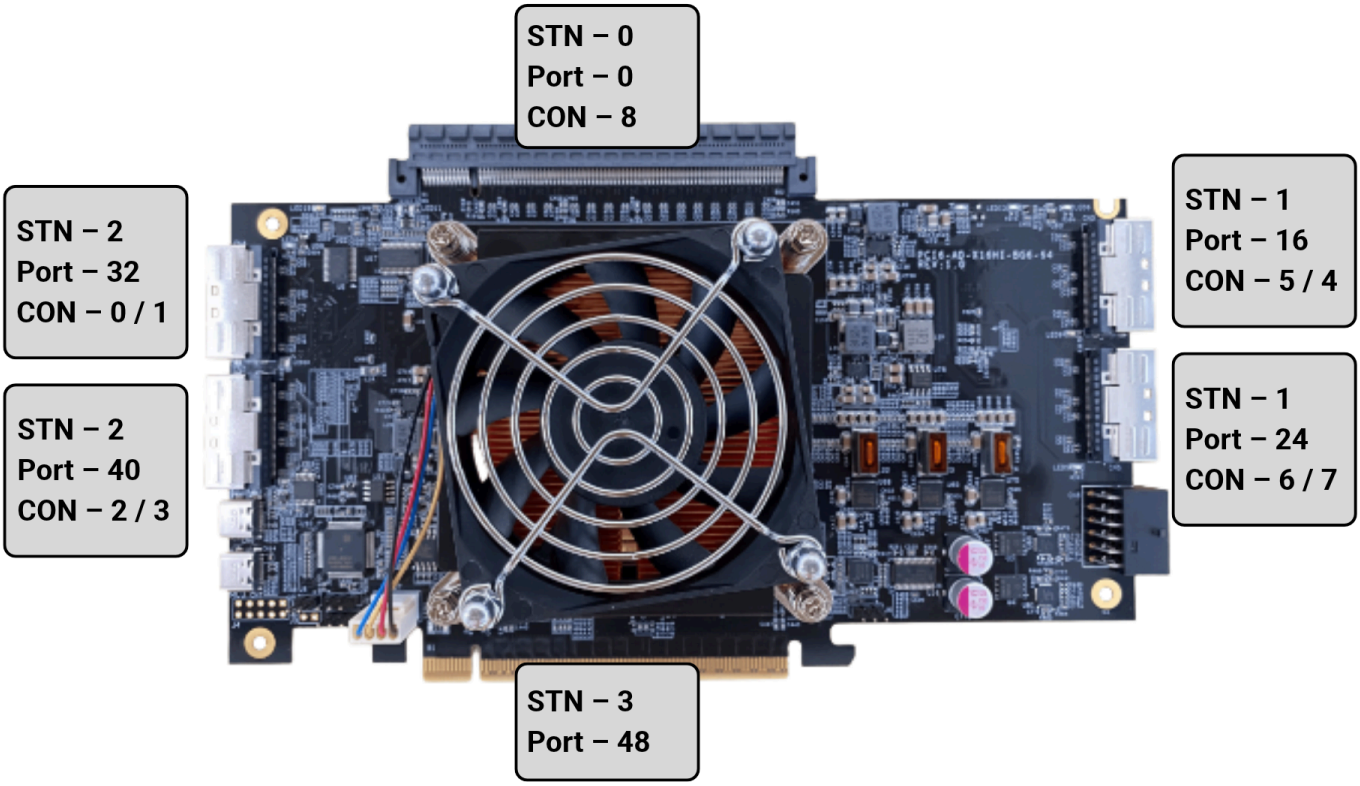


Port and Station Mapping

The Atlas3 64-A0 Host Adapter Card uses station, port, and connector (CON) numbers to identify PCIe interfaces and connected devices. Each station supports up to 16 PCIe lanes, with port assignments corresponding to the switch's internal configuration.

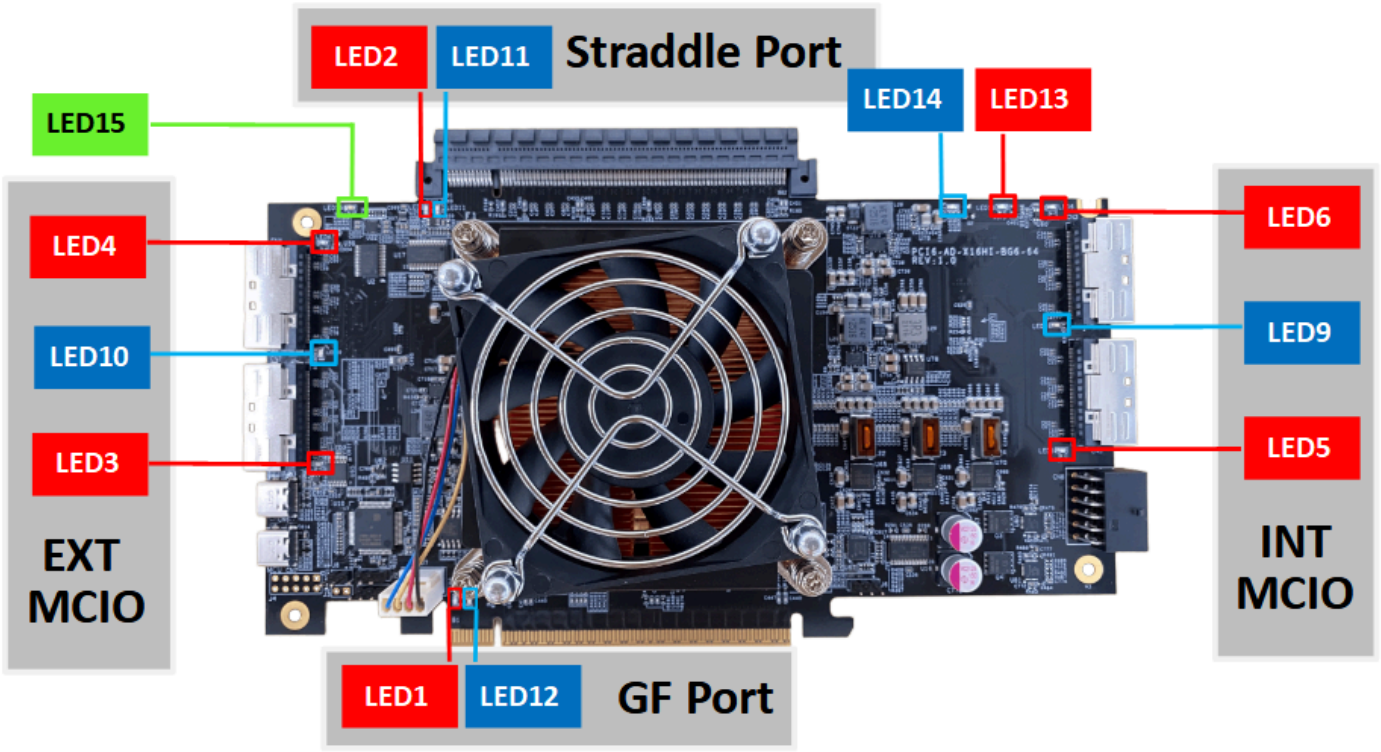
The diagram below identifies the station, port, and CON assignments for the host adapter.

Interface	Station	Port Number	CON Number
PCIe Straddle-Mount	0	0	8
Internal MCIO (upper)	1	16	5 / 4
Internal MCIO (lower)	1	24	7 / 6
External MCIO (upper)	2	32	0 / 1
External MCIO (lower)	2	40	2 / 3
PCIe Golden Finger	3	48	N/A



LED Indicators

The Atlas3 64-A0 Host Adapter Card includes onboard LEDs for monitoring switch status, firmware operation, PCIe link speed, and negotiated link width. The tables below identify each LED and its corresponding function.



System Status LEDs

LED ID	Color	Description
LED13	Red	**System Error Indicator.** Turns on for: • Second expiration of the watchdog timer • Built-In Self-Repair (BISR) error • Firmware signature authentication failure • Double-bit ECC errors
LED14	Blue	**Atlas3 Heartbeat.** Blinks when managed firmware is running normally. Remains solid on when unmanaged firmware is loaded.
LED15	Green	**MCU Status.** Blinks when the MCU firmware is active and responding.

Link Speed LEDs

The Link Speed LEDs (blue) indicate the negotiated PCIe generation for the host, MCIO, and straddle-mount interfaces:

- **Active link** — The LED blink rate corresponds to the negotiated PCIe generation.
- **Gen6 link** — The corresponding LED remains solid.
- **Detailed link status** — Use the **showport** CLI command to view negotiated speed and width.

LED ID	Location	Color
LED12	PCIe Golden Finger	Blue
LED10	External MCIO	Blue
LED9	Internal MCIO	Blue
LED11	PCIe Straddle-Mount	Blue

Link Width LEDs

The Link Width LEDs (red) indicate whether the negotiated PCIe link width matches the expected configuration. The LEDs remain off when the expected link width is achieved.

LED ID	Monitored Port	Color
LED1	PCIe Golden Finger	Red
LED3 / LED4	External MCIO	Red
LED5 / LED6	Internal MCIO	Red
LED2	PCIe Straddle-Mount	Red

Use the **showport** CLI command to compare the desired and negotiated link width for each interface and identify links reported as Active or Degraded.

- A **Degraded** status indicates that the negotiated link speed or width does not match the desired configuration.

Practical Applications and System Integration

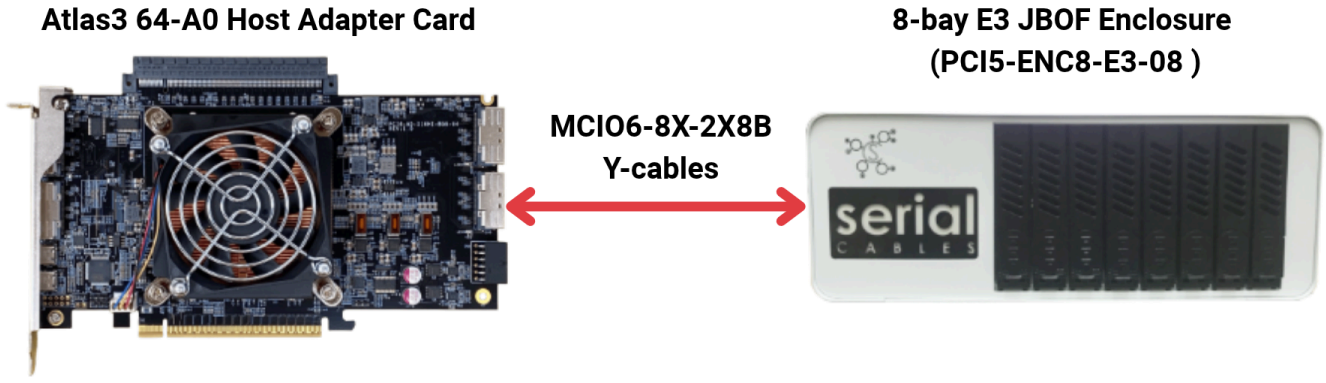
The Atlas3 64-A0 Host Adapter Card supports external PCIe Gen 6 connectivity for storage expansion and add-in card integration. Supported configurations include:

- **Gen 6 JBOF connectivity —** Connect to an external 8-bay E3 JBOF enclosure for access to multiple PCIe SSDs.
- **Direct-attached EDSFF SSDs —** Connect compatible E1.S, E1.L, E2, or E3 SSDs directly through the MCIO interfaces.
- **PCIe slot expansion —** Extend PCIe connectivity to external Gen 6 x16 add-in card slots using compatible MCIO adapters.

Gen 6 JBOF Connectivity

The host adapter can connect to an external JBOF enclosure containing eight single-port x4 E3 SSDs. This configuration provides access to multiple storage devices through the adapter's MCIO interfaces, with Y-cables distributing the PCIe connections to the enclosure.

Component	Description
Host Adapter	Atlas3 64-A0 Host Adapter Card (this product)
Cabling	MCIO6-8X-2X8B Y-cables
Target System	PCI5-ENC8-E3-08 8-bay E3 JBOF enclosure
Storage Devices	Eight single-port PCIe x4 E3 SSDs



Direct-Attached EDSFF SSDs

EDSFF SSDs can be connected directly to the adapter's MCIO interfaces without an external enclosure. This configuration supports individual storage devices in E1.S, E1.L, E2, or E3 form factors.

Component	Description
Host Adapter	Atlas3 64-A0 Host Adapter Card (this product)
Cabling	MCIO6-8X-EDSFFX2-1X4 cable
Target Devices	Compatible E1.S, E1.L, E2, or E3 SSDs

Atlas3 64-A0 Host Adapter Card



MCIO6-8X-EDSFFX2-1X4 Breakout Cable



EDSFF SSDs



PCIe Gen 6 Slot Expansion

The host adapter can extend PCIe connectivity to two external add-in card slots using MCIO-connected expansion adapters. Each expansion adapter provides a physical PCIe x16 slot for compatible add-in cards.

Component	Description
Host Adapter	Atlas3 64-A0 Host Adapter Card (this product)
Cabling	MCIO6-8X-8X-xM cables
Expansion Adapter	Two PCI6-AD-MX8-X16 adapters
Target Devices	Compatible PCIe add-in cards

Command-Line Interface (CLI) Setup

The Atlas3 64-A0 Host Adapter Card includes an onboard microcontroller (MCU) that provides command-line access for switch configuration and diagnostics, as well as firmware management. The card includes two USB Type-C interfaces:

- **CN7** — Primary interface for MCU CLI access and firmware updates.
- **CN6** — Provides Atlas3 I²C slave and selectable SDB/SMART UART access. It is not used for the standard MCU CLI.

The CLI can be used to:

- Monitor temperature, critical voltages, fan speed, power consumption, and PCIe link status.
- Access switch and port registers for configuration and troubleshooting.
- Manage Atlas3 and MCU firmware updates.
- Control PCIe reference clocks and connector reset signals.
- Run board-level diagnostics

Connection Steps

1. Connect a USB Type-C cable between the host computer and the **CN7** connector on the Atlas3 64-A0 Host Adapter Card.

2. After the USB connection is detected, identify the assigned COM port using your system's Device Manager.

3. Open your serial terminal software (Tera Term, PuTTY, or equivalent) and connect to the assigned COM port.

4. A successful serial connection displays the MCU command prompt.

CLI Command Reference

Commands	Description
fdl	Upgrades Atlas3 unmanaged or managed firmware and onboard MCU firmware
lsd	Displays temperature, critical voltages, fan speeds, and board power consumption
mw	Writes a 32-bit value to a specified register within the Atlas3 switch
dr	Dump switch-level registers for diagnostic or debugging purposes
dp	Dumps port-specific switch registers for the selected port
df	Dumps contents of the switch's onboard flash memory
conrst	Sends a PERST# reset pulse to selected MCIO or straddle-mount interfaces
showport	Displays link status and connection details for USP/DSP ports
bist	Runs the onboard Built-In Self-Test (BIST) for device diagnostics
setmode	Configures the SBR reference-clock and Gen6 precoding mode
showmode	Displays the current clock mode of the host card
spread	Configures the PCIe clock spread spectrum setting
clk	Enables or disables the PCIe clock output
sdb	Sets the MCU SDB port state (on/off)
uart	Selects the CN6 UART path between SMART UART and the Atlas3 SDB interface
pwr	Displays the status of the onboard power regulators
counters	Displays error counters and statistics for all active ports
flit	Configures PCIe Gen 6 FLIT mode settings
iicwr	Performs an I²C/SMBus write-read transaction
iicw	Performs an I²C/SMBus write transaction
i3cwr	Performs an I3C write-read transaction
i3cw	Performs an I3C write transaction
i3cr	Performs an I3C read transaction
i3c_ccc	Sends I3C Common Command Code (CCC) operations
mctp	Executes Management Component Transport Protocol (MCTP) commands
packet	Executes packet-related operations
ver	Displays version information for the host card, MCU firmware, and Atlas3 firmware
sysinfo	Displays system configuration, firmware information, power status, PCIe link state, and onboard diagnostics
reset	Performs reset operations for the onboard MCU, PCIe hierarchy, or Atlas3 switch

Command Usage Notes

Firmware Upgrade and Management – fdl

The **fdl** command is used to upgrade the Atlas3 firmware, including unmanaged switch firmware, managed firmware, and MCU firmware. Firmware is transferred over the serial interface using the XMODEM protocol.

Enter the command **fdl** followed by the target upgrade mode. There are four to choose from:

- **mini** – Updates the unmanaged mini SBR firmware.
- **main** – Updates the unmanaged main SBR firmware.
- **fw** – Updates the managed switch firmware.
- **mcu** – Updates the on-board MCU firmware.

When executed, the system prompts for confirmation before erasing and writing flash memory.
Press **Y** to continue or **Ctrl+X** to cancel.

The **mini**, **main**, and **fw** commands erase all regions of the Atlas3 switch flash before the new firmware is written.

Firmware Upload Procedure

Step 1 – Connect via Serial Interface

- Connect a USB-C cable to the host card's **CN7** port.
- Identify the COM port in your system's **Device Manager**.
- Open a terminal emulator such as **TeraTerm/puTTy** (Windows) or **minicom** (Linux) and connect to that COM port.
- A successful connection will display the command prompt (Cmd>).

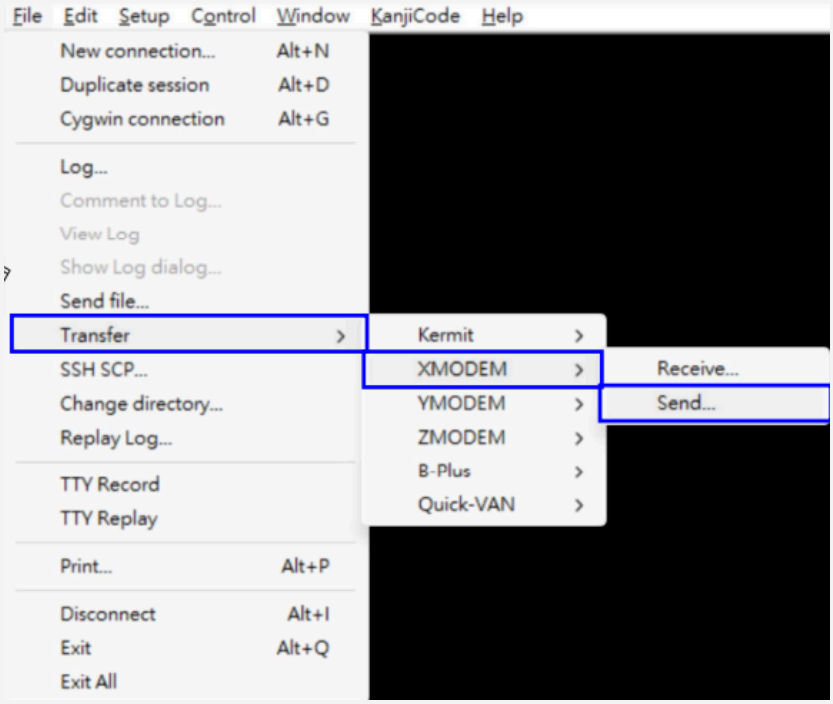
Step 2 – Run the Upload Command

1. Enter the appropriate **fdl** command (e.g., **fdl main**).
2. When prompted, press **Y** to confirm the upgrade or **Ctrl+X** to cancel.
3. The flash memory will be erased, and the system will wait for incoming data via XMODEM.

Continued on the next page.

Step 3 – Send the Firmware File via XMODEM

- In **TeraTerm** – Go to **File** → **Transfer** → **XMODEM** → **Send**, then select the **BIN firmware file**.



- In **minicom** – Use **Send File** → **XMODEM** and choose the **BIN firmware file**.

Step 4 – Apply the New Firmware

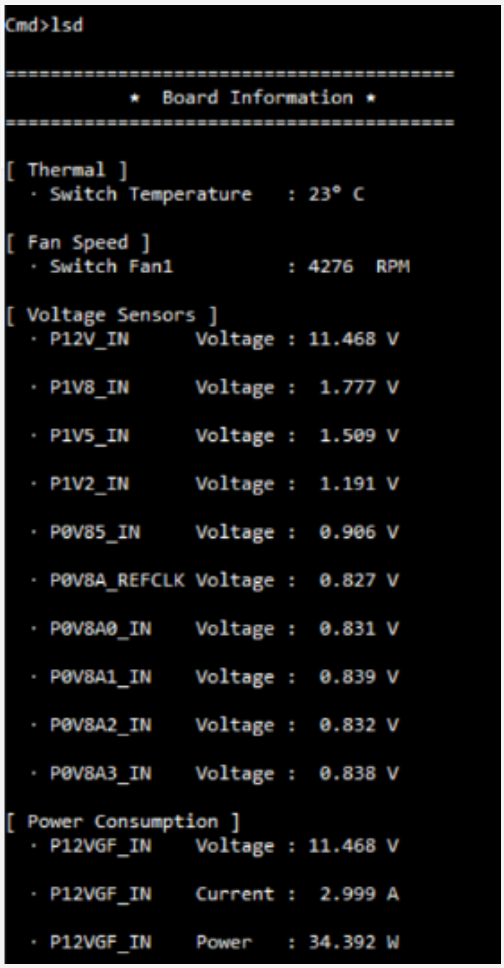
- After the upload finishes, power cycle the host card for unmanaged or managed firmware updates. For MCU firmware upgrades, use the **reset** command instead of a power cycle to activate the new MCU firmware.

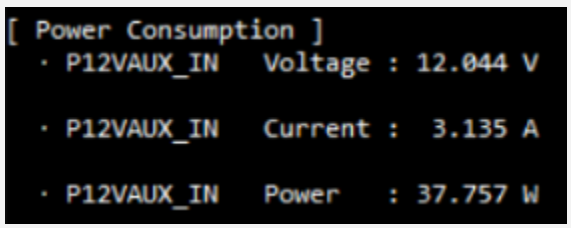
System Diagnostics (Sensors and Power) – lsd

The **lsd** command displays real-time system diagnostics for the Atlas3 64-A0 Host Adapter Card, including temperature, fan speed, voltage readings, and power consumption. This information helps monitor board health, identify abnormal conditions, and verify proper cooling and power delivery.

The output includes:

- **Thermal** – Reports the temperature near the Atlas3 PCIe switch.
- **Fan Speed** – Shows the host card fan RPM
- **Voltage Sensors** – Reports monitored onboard rails, including **P12V_IN**, **P1V8_IN**, **P1V5_IN**, **P1V2_IN**, **P0V85_IN**, **P0V8A_REFCLK**, and the monitored **P0V8A0_IN** through **P0V8A3_IN** rails.
- **Power Consumption** – Reports voltage, current, and power readings for the host card's 12 V input. When powered through the PCIe golden finger, readings are reported under **P12VGF_IN**. When powered through the auxiliary 12 V connector, readings are reported under **P12VAUX_IN**.





Register Write – mw

The **mw** command writes a 32-bit value to a specific register address within the Atlas3 PCIe switch. It writes the specified hexadecimal data directly to the target register for switch configuration and low-level hardware control.

Enter the command **mw** followed by the register address (hex) and the data value (hex) to be written. Valid register addresses range from **0x00000000** to **0xFFFFFFFC**, and writable data values range from **0x00000000** to **0xFFFFFFFF**. For example:

- **mw fff0017c ffffffff** – This writes the data **0xFFFFFFFF** to the register address **0xFFF0017C** on the Atlas3 switch

Switch Register Dump – dr

The **dr** command reads and dumps switch-wide register values from the Atlas3 PCIe switch.
It retrieves low-level register data across the switch's address space for debugging, validation, and hardware bring-up.

Enter the command **dr** followed by the starting register address (hex) and an optional count (hex) to specify how many bytes to read. The valid register addresses and count values range from **0x00000000** to **0xFFFFFFFC**. For example:

- **dr 60800000** – Dumps Atlas3 switch register values beginning at 0x60800000 (PCIe straddle-mount, Port 0)

Register Address Mapping

Each port's register block is separated by an offset of 0x8000. The following base addresses apply to the active PCIe interfaces on this card:

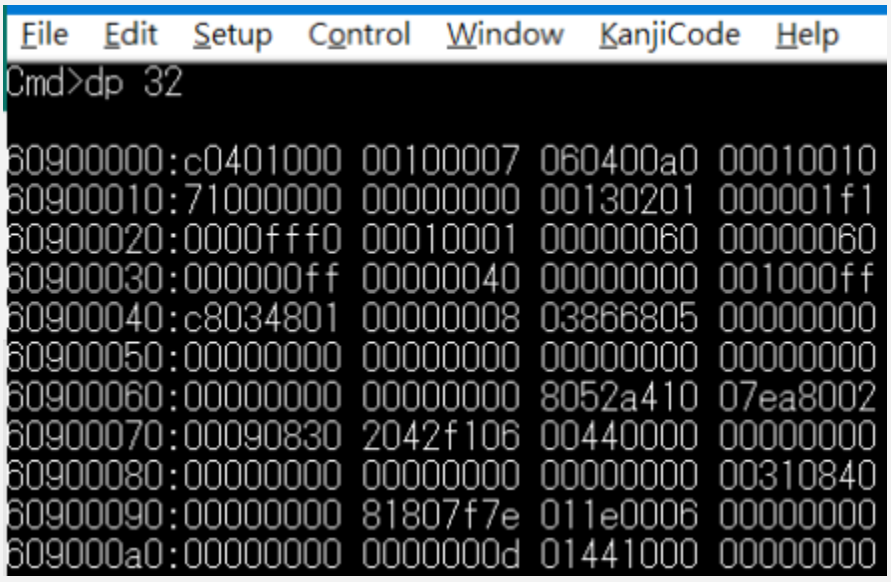
Interface	Port	Base Address
PCIe Straddle-Mount	0	0x60800000
Internal MCIO	16	0x60880000
External MCIO	32	0x60900000
PCIe Golden Finger	48	0x60980000

Port Register Dump – dp

The **dp** command reads and dumps port-specific register values from the Atlas3 PCIe switch.
It displays low-level hardware data for a selected physical port and is primarily used for port-level debugging and validation.

Enter the command **dp** followed by the port number (0–111) to dump switch registers for that port. For example:

- **dp 32** – Dumps switch register values for Port 32.



Refer to **Port and Station Mapping** for physical port assignments.

Flash Dump — df

The **df** command reads and dumps the contents of the switch flash memory to the console or a connected host interface. It retrieves raw flash data for firmware inspection, debugging, or verification.

Enter the command **df** followed by the start address (hex) and optionally the byte count (hex) to dump data from the switch flash memory. Both the address and count can range from 0x00000000 to 0xFFFFFFFC. For example:

- **df 400** – Dumps the flash contents starting from address 0x00000400
- **df 400 4** – Dumps 4 bytes of flash data starting from address 0x00000400

Connector Reset — conrst

The `conrst` command sends a 300 ms PERST# reset pulse to connected MCIO devices or the PCIe straddle-mount interface.

If the `conrst` command is entered with a connector number (0–8) or `all`, the CLI sends a reset signal to the specified connector(s) and optional channel (`a` or `b`). For example:

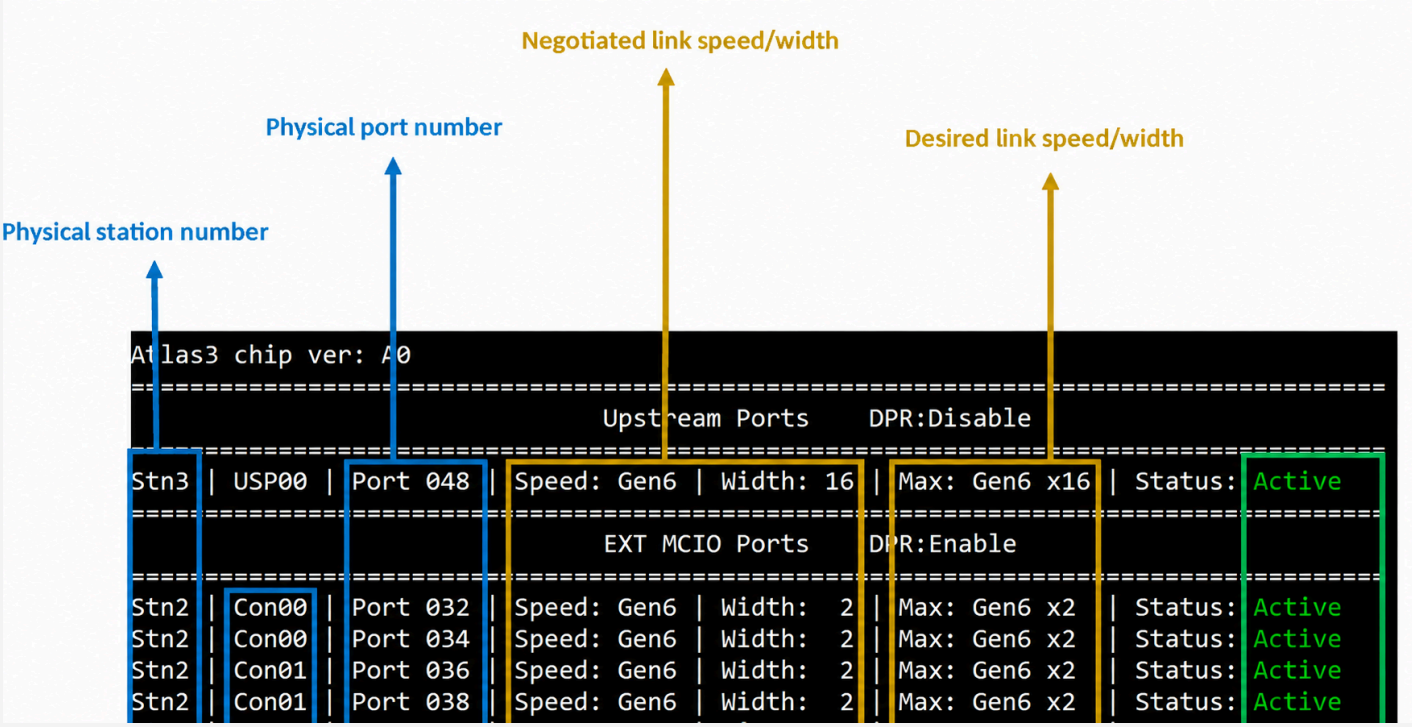
- `conrst 1` — Sends a PERST# reset to connector 1
- `conrst all` — Sends a PERST# reset to all connectors
- `conrst all a` — Sends a PERST# reset to channel a of all connectors

Note:

- Channel a uses PERST# signals on **MCIO pins B11/B12**
- Channel b users PERST# on **MCIO pins B29/B30**

Port Link Status– showport

The **showport** command displays the link status for all upstream (USP) and downstream (DSP) ports on the Atlas3 PCIe switch. The output shows each port's station number, connector or upstream-port identifier, physical port number, negotiated link speed and width, desired link speed and width, and current link status:



Output Field Descriptions

Field	Description
Station Number	Physical station index on the Atlas3 switch.
Connector / Port ID	Identifies the MCIO connector, straddle-mount interface, or upstream PCIe port associated with the physical port.
Physical Port Number	Physical switch port number assigned to the interface.
Speed	The **negotiated PCIe generation** (e.g., Gen1, Gen4, Gen6).
Width	The **negotiated link width** (e.g., x1, x4, x8, x16).
Max	The **desired PCIe link** speed and width for the port.
Status	Current link condition (Active, Idle, or Degraded).
DPR	Shows whether Dynamic Port Reconfiguration (DPR) is enabled for the port group.

Status Definitions

- **Degraded** – Link trained successfully but negotiated speed or width is lower than expected.
- **Idle** – No physical link detected or device not present on the port.
- **Active** – Desired and negotiated link speed/width matched successfully.

Dynamic Port Reconfiguration (DPR)

Dynamic Port Reconfiguration (DPR) allows the internal and external MCIO interfaces to support different PCIe link widths, including multiple x2 connections, without requiring a full switch reset.

Built-In Self-Test — bist

The **bist** command runs a basic diagnostic routine on the Atlas3 64-A0 Host Adapter Card. It checks communication with onboard I²C devices and reports the status of each detected component.

The diagnostic covers devices such as power regulators, EEPROM, I²C I/O expanders, I²C multiplexers, clock generators, and clock buffers.

The test runs automatically once invoked and reports **OK** or **FAIL** results for each test item:

Channel	Device	Address	Status
CH0	PCA9575-0	0x40	OK
CH0	PCA9575-1	0x42	OK
CH0	PCA9575-2	0x44	OK
CH0	MP2971	0xBE	Fail
CH0	AT24C16	0xA0	OK
CH0	TMP112	0x92	OK
CH3	PCA9548	0xE2	OK
CH1	RC21012	0x12	OK
CH1	RC19016	0xD8	OK

Host Card Mode Configuration — setmode

The **setmode** command selects the Serial Boot Record (SBR) configuration used by the Atlas3 64-A0 Host Adapter Card. Each mode defines the PCIe reference-clock configuration and whether Gen 6 precoding is enabled.

Enter the command **setmode** followed by the mode number (1–5) to configure the host card's operating mode. The controller must be reset for the change to take effect:

Mode	Description
1 – Common Clock / Precoding Enabled	Uses a common reference clock between the host and switch, with Gen 6 precoding enabled.
2 – Common Clock / Precoding Disabled	Uses a common reference clock between the host and switch, with Gen 6 precoding disabled.
3 – SRNS / Precoding Enabled	Uses Separate Reference Clocks with No Spread (SRNS), with Gen 6 precoding enabled.
4 – SRNS / Precoding Disabled	Uses Separate Reference Clocks with No Spread (SRNS), with Gen 6 precoding disabled.
5 – Reserved	Reserved for future use.

Show Host Card Mode — showmode

The **showmode** command displays the current operating mode of the Atlas3 64-A0 Host Adapter Card. Use it to verify the active PCIe reference-clock and precoding configuration after running **setmode**.

PCIe Clock Spread Setting – spread

The **spread** command configures spread-spectrum behavior for the Atlas3 PCIe reference clock. It can operate with spread disabled or with down-spreading of 3,000 ppm or 5,000 ppm.

Enter the command **spread** followed by the **1**, **2**, or **off**:

Command	Clock Behavior
spread 1	3,000 ppm down-spread (-0.3%)
spread 2	5,000 ppm down-spread (-0.5%)
spread off	Spread spectrum disabled

PCIe Clock Output Control – clk

The **clk** command enables or disables PCIe reference clock outputs to the straddle-mount and internal/external MCIO connectors. These clocks provide timing signals to connected PCIe devices during link initialization and operation. Disabling the outputs does not affect the Atlas3 switch's own system reference clock.

This allows engineers to control downstream clock delivery independently when bringing up or troubleshooting connected PCIe devices.

- **clk en** – Enables PCIe reference clock outputs to the straddle-mount and MCIO interfaces.
- **clk dis** – Disables PCIe reference clock outputs to the straddle-mount and MCIO interfaces.

Clock Output Guidelines

- Clock output can be changed dynamically and does not require a host card power cycle.
- The setting is stored in the MCU and applied automatically the next time the host card powers on.
- The Atlas3 switch system reference clock remains enabled regardless of the downstream clock-output setting.

SDB Port Control — sdb

The **sdb** command enables or disables the Atlas3 Serial Debug Bridge (SDB) interface. It determines whether the board remains in normal MCU-controlled CLI operation or makes the SDB interface available for external Broadcom debug utilities.

Enter the command **sdb** followed by **off** or **on**:

Command	Description	Typical Use
sdb off	Sets the MCU SDB state to OFF.	Used for **normal operation** like running CLI commands such as **fdl**, **mw**, **dr**, **dp**, and **showport**.
sdb on	Sets the MCU SDB state to ON.	Used for **utility mode** – running host-based tools such as **SwitchCLID** or **ARCTIC** from a PC.

SDB Behavior Notes

- Only one mode is active at a time (normal MCU/CLI operation or SDB utility access).
- Setting **sdb on** switches the board from normal MCU/CLI operation to SDB access for host-based utilities.

Utilities such as SwitchCLID and ARCTIC are Broadcom-provided tools distributed under NDA and SLA. Contact Broadcom for licensing, access, or additional support information.

UART Path Selection — uart

The **uart** command selects the UART path for the **CN6** (USB Type-C) interface, switching between the Atlas3 SDB (Serial Debug) interface and the SMART UART interface.

Enter the command **uart** followed by **0** or **1**:

- **uart 0** – Routes CN6 to SMART UART
- **uart 1** – Routes CN6 to SDB (default)

UART Path Notes

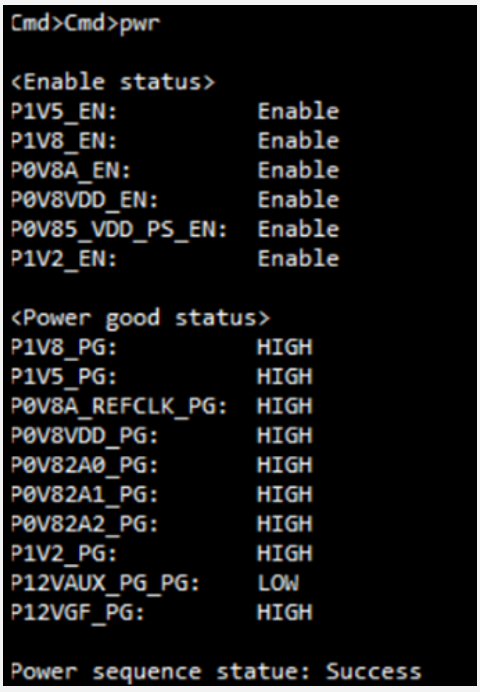
- The selected UART path is stored and applied after a power cycle.
- SDB (Serial Debug) is supported in both managed and unmanaged firmware modes.
- SMART UART is supported only in managed firmware mode.

Power Status — pwr

The **pwr** command displays the current power status of the Atlas3 64-A0 Host Adapter Card, including power-rail enable states, power-good signals, and overall power sequencing status. A “Success” power sequence status indicates all required rails initialized correctly.

The output is organized into:

- **Enable Status** — Shows whether each monitored power rail is enabled or disabled.
- **Power Good Status** — Reports the power-good state for each monitored rail.
- **Power Sequence Status** — Reports whether the board power-up sequence completed successfully.



Port Error Counters — counters

The **counters** command displays error counters for each active port on the Atlas3 PCIe switch. The output includes **PortRx**, **BadTLP**, **BadDLLP**, **RecDiag**, **LinkDown**, and **FlitError** counters, providing a quick view of link and protocol-level errors across the switch.

- **counters** – Displays the current error counts for all ports.
- **counters clear** – Clears the error counters for all ports.

About Error Counter Behavior

- The FLIT error counter increments by 1 when enabled and a countable event occurs, as defined by the FLIT Error Counter Control Register.
- If non-zero, the counter decrements at a fixed rate based on the link encoding and width.
- The counter is cleared when the FLIT Error Counter Enable bit transitions from **0b** to **1b**.

FLIT Mode Control — flit

The **`flit`** command controls FLIT disable mode on Atlas3 PCIe ports. The setting determines whether a port advertises FLIT mode support during PCIe link training.

Enter **`flit`** followed by either **all** or a station ID (0–3), then specify **on** or **off**. Enter **flit** by itself to view which stations are enabled and which are disabled. For example:

- **flit 2 off** – Clears the FLIT-disable setting for station 2 (external MCIO), allowing FLIT support to be advertised
- **flit all on** – Enables FLIT-disable mode for all stations, preventing FLIT support from being advertised during link training

Station IDs follow the host card station mapping defined in **Port and Station Mapping**. For the 64-A0, valid station IDs are 0, 1, 2, and 3.

About FLIT Disable Mode

- Enabling FLIT disable mode prevents the port from advertising FLIT support during link training.
- This setting does not modify the FLIT capability reported in PCIe configuration registers.
- FLIT mode is required for operation at 64 GT/s (Gen6). Disabling FLIT will prevent links from training at Gen6 speeds.

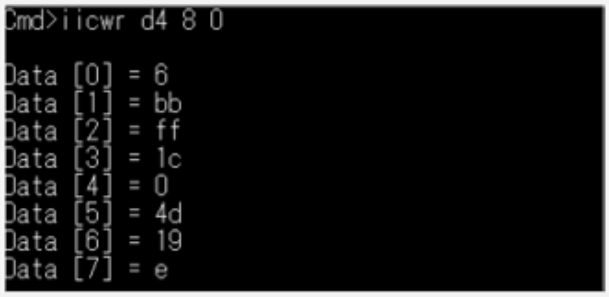
SMBus Read — iicwr

The **iicwr** command reads SMBus data from devices connected through the MCIO interfaces. It can be used to access device registers for diagnostics or validation.

Enter **iicwr** followed by the device address (hex), connector number (0–8), read length (up to 128 bytes), and starting register offset (hex).

For example:

- **iicwr d4 0 8 0** – Reads 8 bytes from SMBus device address 0xD4, starting at register 0x00 on connector 0.



- Channel A uses the I²C interface on MCIO pins B8/B9.
- Channel B uses the I²C interface on MCIO pins B26/B27.

SMBus Write — iicw

The **iicw** command writes SMBus data to devices connected through the MCIO interfaces. It is typically used to write register values or configuration data to attached devices.

Enter the command **iicw** followed by the device address (hex), connector number (0–8), and one or more data bytes (hex) to be written. The maximum write length is 128 bytes. For example:

- **iicw d4 ff** – Writes 0xFF to the device at SMBus address 0xD4 on connector 0



I3C Write/Read – i3cwr

The `i3cwr` command performs an I3C write/read transaction with a device connected to the PCIe straddle-mount interface (**CN1**). Communication uses the fixed I3C Channel 8.

Enter `i3cwr` followed by the device address (hex), number of bytes to read (up to 128), and one or more write-data bytes (hex). The maximum write length is 128 bytes. For example:

- `i3cwr 30 8 0` – Writes 0x00 to the I3C device at address 0x30, then reads 8 bytes from the device

I3C Write – i3cw

The `i3cw` command writes data to an I3C device connected through the PCIe straddle-mount interface (**CN1**). Communication uses the fixed I3C Channel 8.

Enter `i3cw` followed by the device address (hex) and one or more write-data bytes (hex). The maximum write length is 128 bytes. For example:

- `i3cw 30 0 ff` – Writes 0x00 and 0xFF to the I3C device at address 0x30

I3C Read – i3cr

The `i3cr` command reads data from an I3C device connected through the PCIe straddle-mount interface (**CN1**). Communication uses the fixed I3C Channel 8.

Enter `i3cr` followed by the device address (hex) and the number of bytes to read (up to 128). For example:

- `i3cr 30 8` – Reads 8 bytes from the I3C device at address 0x30

I3C Common Command Codes – i3c_ccc

The **i3c_ccc** command executes I3C Common Command Codes (CCCs) defined in the MIPI I3C Basic v1.1.1 specification. It supports device discovery and configuration through the fixed I3C Channel 8 (PCIe straddle-mount interface, CN1).

Enter **i3c_ccc** followed by a command name or hexadecimal CCC ID, the target device address (hex) when required, and any associated data bytes (hex). Use **i3c_ccc -h** to display additional command options. For example:

- **i3c_ccc SETDASA 50 30** – Assigns dynamic address 0x30 to a device at static address 0x50
- **i3c_ccc RSTDAA** – Resets dynamic address assignments
- **i3c_ccc ENTDAA 30** – Initiates dynamic address assignment, starting at 0x30
- **i3c_ccc GETPID 30** – Reads the Provisional ID (PID) of a device at address 0x30
- **i3c_ccc SETNEWDA 30 35** – Changes a device's dynamic address from 0x30 to 0x35

```
Cmd>i3c_ccc ENTDAA 30

Success: [ENTDAA] (ID: 0x07, Assigned DA: 0x30)

--- [ENTDAA Captured Target Characteristics] ---
Raw Data:
  - PID : 0x02 0x36 0x15 0x2A 0x00 0x90
  - BCR : 0x03
  - DCR : 0x63

[PID Breakdown Analysis]
  - [47:33] MIPI Manufacturer ID : 0x011B
  - [32]    PID Type Selector    : 0x0 (Vendor-fixed Value)
  - [31:16] Part ID              : 0x152A
  - [15:12] Instance ID          : 0x0
  - [11:0]  Extra Info           : 0x090

[BCR Breakdown Analysis: 0x03]
  - [7:6] Device Role          : I3C Target (Slave)
  - [5]   Advanced Capabilities: Not Supported
  - [4]   Virtual Target       : Physical Target
  - [3]   Offline Capable      : No
  - [2]   IBI Payload          : No Data Byte
  - [1]   IBI Request Capable  : Capable (Interrupt Support)
  - [0]   Max Speed Limitation : Limitation Exists (See GETMXDS)

[DCR Breakdown Analysis: 0x63]
  - Device Class / Type  : 0x63
Cmd>
```

MCTP Command – mctp

The **mctp** command sends Management Component Transport Protocol (MCTP) commands to connected devices. It supports device identification, health monitoring, and management operations through the selected slot.

Enter `mctp` followed by the slot number (0–8) and one of the supported operations: **sn**, **health**, **pause**, **resume**, **abort**, **status**, **or replay.** For example:

- `mctp 1 sn` – Requests the serial number of the device in slot 1
- `mctp 1 health` – Requests health status information from the device in slot 1

MCTP Packet – packet

The **packet** command sends raw Management Component Transport Protocol (MCTP) packet data to a device in the selected slot. It allows users to transmit hexadecimal packet data for device communication and debugging.

Enter **packet** followed by the slot number (0–8) and the packet data (hex). The maximum packet length is 128 bytes. For example:

- `packet 8 3a f 11 21 1 0 0 fc 84 0 0 0 4 45 0 0 cd 21 ec 1e c1` – Sends the specified hexadecimal packet data to slot 8

System Version — ver

The **ver** command displays host card identification and version information for the MCU and Atlas3 switch. Use it to verify the running firmware and switch mode before or after a firmware update.

---------- Product Info ----------	
Company :	Serial Cables
Model :	PCI6-AD-x16HI-BG6-64
Serial No. :	
---------- App Info ----------	
Version :	0.0.2
Build Time :	Oct 13 2026 19:52:38
---------- SBR Info ----------	
Version:	0164A00B
Switch Mode:	Unmanaged mode

System Information — sysinfo

Displays a complete summary of the Atlas3 64-A0 Host Adapter Card's configuration and operating status, including firmware information, board telemetry, power status, PCIe link state, clock configuration, and onboard device diagnostics.

This is effectively a sequence of several key commands consolidated into a single report for quick system validation.

System Reset — reset

The **reset** command provides several reset functions for the Atlas3 64-A0 Host Adapter Card. It can reset the onboard MCU, reset a PCIe hierarchy through its PERST# signal, or send a system power-on reset to the Atlas3 switch.

Enter the command **reset** followed by an optional reset type to control how the host card is reset. For example:

- **reset** – Reset the onboard MCU
- **reset s0** – Resets the S0 PCIe hierarchy through **S0_PCE_PERST_N**
- **reset sw** – Sends a system power-on reset (**SYS_PWR_ON_RST_N**) to the Atlas3 PCIe switch

The **reset** command can also be used after an MCU firmware update to activate the new firmware without power cycling the host card.

Maintenance and Diagnostics

The Atlas3 64-A0 Host Adapter Card includes CLI commands and onboard indicators for monitoring system health and PCIe connectivity. The following checks can help identify common issues during installation, testing, or troubleshooting.

- **For a general system check**, run **sysinfo** to collect firmware information, board telemetry, power status, PCIe link state, clock configuration, and onboard device diagnostics in a single report.

- **If a PCIe link does not train as expected**, run **showport** to compare the negotiated and desired link speed and width. A **Degraded** status indicates that the negotiated speed or width does not match the desired configuration. Use **counters** to check for accumulated port errors.

- **If a power issue is suspected**, run **pwr** to check power-rail enable states, power-good signals, and sequencing status. Use **lsd** to review voltage readings and power consumption.

- **If the Atlas3 System Error LED (LED13) is illuminated**, run **bist** to check communication with onboard I²C devices and **lsd** to review temperature, voltage, fan speed, and power telemetry.

- **After a firmware update**, run **ver** to confirm the installed MCU and Atlas3 firmware versions. Atlas3 managed or unmanaged firmware updates require a host-card power cycle, while an MCU firmware update can be applied using the **reset** command.

Revision History

Revision	Description
1.1	Reformatted and restyled for brand consistency and readability. Rewritten for clarity. Added *Product Overview*, *Safety, Handling & Compliance*, *Maintenance & Diagnostics,* and *Contact Us* sections.
1.0	Initial manual release.

Contact Us

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