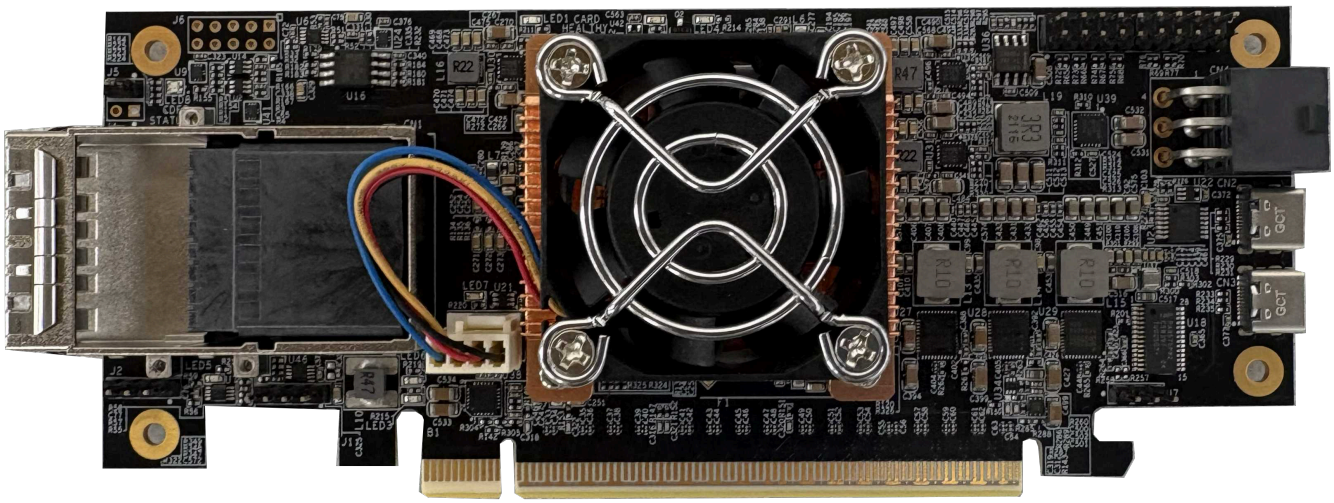
SERIAL CABLES

PCIe 6.0 CDFP HHHL Host Card

TECHNICAL MANUAL



Revision 1.2 Aug 2026

PCI6-AD-x16HE-CDFP-BG6

Command-line interface for monitoring

PCI EXPRESS 6.0

CXL Compute Express Link™

Serial Cables LLC.

Phone: (303) 495-2320 Email: sales@serialcables.com https://serialcables.com

Table of Contents

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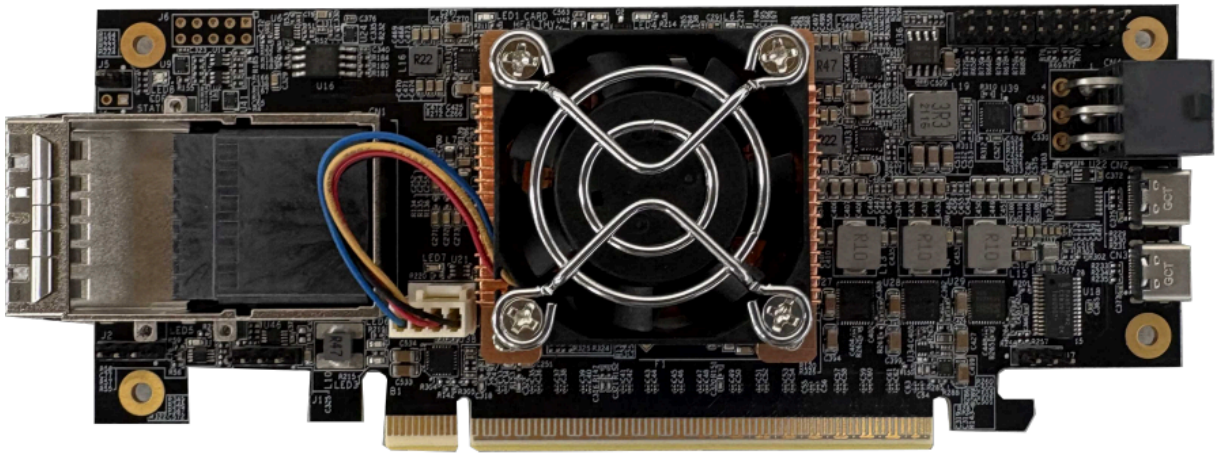
Product Overview

The Serial Cables Atlas3 CDFP Host Adapter Card is a PCIe Gen6 switch-based platform for connecting a host system to PCIe devices and expansion hardware through a CDFP x16 interface. Built around the Broadcom Atlas3 PEX90032 switch, the card supports up to 32 PCIe lanes and 16 ports with flexible port configuration.

A right-angle CDFP x16 (SFF-TA-1032) connector provides the external PCIe interface for host-to-target connections. The card can be paired with CDFP cabling or compatible CDFP adapter hardware to extend PCIe Gen6 connectivity outside the host system.

An onboard microcontroller (MCU) provides direct management through USB Type-C. The CLI can monitor board conditions, inspect switch and port registers, control CDFP functions, check PCIe link status, and perform firmware updates. The Atlas3 switch supports both unmanaged operation and managed operation with firmware.



Key Features

- **Broadcom Atlas3 PCIe Gen6 Switch (PEX90032)** — Supports up to 32 PCIe lanes and 16 ports with flexible port configuration.
- **CDFP x16 Connectivity** — Right-angle SFF-TA-1032 CDFP x16 connector provides a high-speed PCIe Gen6 interface for compatible cables and downstream hardware.
- **Managed and Unmanaged Firmware Modes** — Supports unmanaged switch operation as well as managed operation with Atlas3 firmware.
- **Integrated MCU and USB-C Management Control** — Onboard MCU provides CLI access for configuration, firmware updates, board monitoring, and troubleshooting.
- **Onboard Diagnostics** — CLI commands provide access to temperature, critical voltages, fan speed, power consumtion, PCIe link state, port registers, and error counters.
- **Advanced Atlas3 Switch Functions** — Supports NT ports, DMA channels, peer-to-peer data transfer, hot-plug operation, and FLIT/FEC functionality.

Safety, Handling, and Compliance

The Atlas3 CDFP Host Adapter Card is intended for use in PCIe systems, test platforms, and engineering environments. Installation and handling should be performed by personnel familiar with PCIe hardware and ESD-safe procedures.

Improper installation, inadequate power delivery, or restricted airflow can interfere with normal operation or damage connected hardware.

Electrical Safety

The Atlas3 CDFP Host Adapter Card receives power from two sources:

- **PCIe interface** — Supplies power to the host adapter card and onboard components.
- **CN4 6-pin 12 V connector** — Supplies additional 12 V power to pin B29 of the CDFP connector for attached hardware that requires it.

The host card can consume up to 42 W under Gen6 x32 operation, including fan power. This figure does not include 12 V power supplied through the CDFP interface for connected AOC or AEC cables.

Before installation:

- Power down the host system and disconnect external power before installing or removing the card.
- Verify that the system provides sufficient power for the host adapter and connected CDFP hardware.
- Confirm that CN4 is connected when the attached CDFP device or cable requires the 12 V supply.
- Avoid connecting or disconnecting the host card, CDFP cable, or auxiliary power connection while the system is energized.

ESD Protection

The host adapter contains components that can be damaged by electrostatic discharge.

- Work only in an electrostatic discharge-safe area with a grounded mat and wrist strap.
- Keep the card in its anti-static packaging until you are ready to install it.
- Avoid touching connector pins, exposed traces, or any metallic contacts.

Thermal and Airflow Considerations

The board includes an onboard heatsink and fan assembly and requires proper airflow for stable operation:

- Maintain clear airflow around the card.
- Do not obstruct the fan or heatsink.
- Operate the adapter only within an ambient temperature range of 0 °C to +40 °C.

Compliance

This product is manufactured in accordance with standard international safety and environmental regulations:

- **CE** – Conforms to applicable European EMC and low-voltage directives.
- **FCC Class A** – Intended for use in commercial or industrial environments.
- **RoHS 3** – Compliant with the Restriction of Hazardous Substances directive.

Hardware Specifications

The Atlas3 CDFP Host Adapter Card is a PCIe Gen6 switch board built around the **Broadcom PEX90032**. It provides a PCIe host connection through the card edge and a **CDFP x16 interface** for connecting external PCIe hardware.

An onboard MCU provides management and diagnostic access through USB Type-C, including switch configuration, firmware updates, telemetry, and link monitoring.

Parameter	Specification
PCIe Interface	PCIe Gen6 x16 edge connector (golden finger)
External PCIe Interface	1 × right-angle CDFP x16 (SFF-TA-1032) connector
Switch Device	Broadcom PEX90032 PCIe Gen6 Switch
Total PCIe Lanes	Up to 32 lanes
Active PCIe Interfaces	Golden-finger x16 + CDFP x16
Firmware Modes	Managed and unmanaged
Management Interfaces	2 x USB Type-C
Maximum Board Power	42 W maximum, including fan power; excludes 12 V power supplied to the CDFP interface
CDFP Auxiliary Power	CN4 6-pin 12 V connector; supplies CDFP connector pin B29
Operating Temperature	0 °C to +40 °C ambient
PCB Dimensions	167 mm (L) × 69 mm (H) × 44 mm (T), including heatsink

Power Requirements

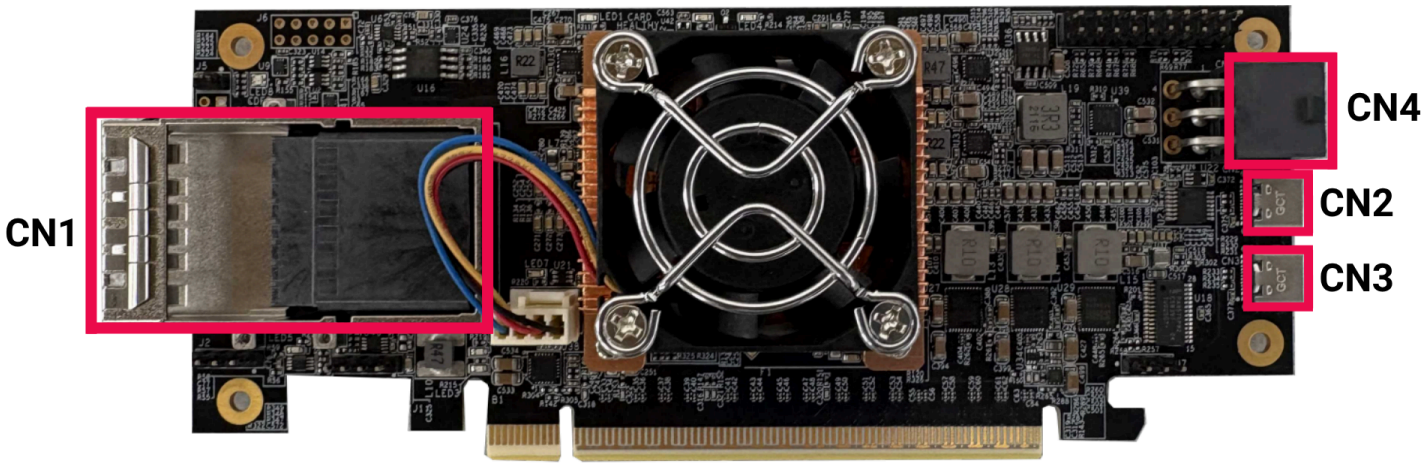
The Atlas3 CDFP Host Adapter Card uses separate power paths for the host adapter and the CDFP interface:

- **PCIe edge connector** – Supplies operating power to the host adapter and its onboard components
- **CN4 6-pin 12 V connector** – Provides a separate 12V supply to pin B29 of the CDFP connector for connected CDFP hardware.

Connector Locations and Functions

The Atlas3 CDFP Host Adapter Card includes four primary external connectors for PCIe connectivity, board management, debug access, and CDFP power. Connector designators are silk-screened on the PCB.

Designator	Connector Type	Function / Description
CN1	CDFP x16 (SFF-TA-1032) Connector	Provides the card's external PCIe Gen6 x16 interface for connection to compatible CDFP cables and PCIe hardware.
CN2	USB Type-C Connector	Provides access to the Atlas3 SDB and SMART UART interfaces. Two COM ports are exposed through the USB connection.
CN3	USB Type-C Connector	Primary MCU management interface used for CLI access, board configuration, diagnostics, and firmware updates.
CN4	6-Pin 12 V Power Connector	Supplies 12 V power to pin B29 of the CDFP connector for attached CDFP hardware requiring auxiliary power.



CN1 – CDFP x 16 Connector

CN1 is a right-angle **CDFP x16 SFF-TA-1032** connector that provides the external PCIe Gen6 interface for the host adapter. The connector carries a PCIe x16 link along with the associated clock, reset, management, and power signals defined by the card implementation.

This manual provides the complete 120-pin connector definition, including:

- PCIe transmit and receive differential pairs for lanes 0–15
- Reference-clock and reset signals
- I²C sideband signals
- 3.3 V and 12 V power connections
- Ground and auxiliary sideband signals

CN1 Root-Complex End Pinout

The following tables list the CN1 CDFP x16 connector pin assignments at the root-complex end. Pins are organized by connector rows A through D and positions 1 through 30.

	1	2	3	4	5	6
A	GND	PETP12	PETN12	GND	PETP13	PETN13
B	GND	PETP11	PETN11	GND	PETP10	PETN10
C	GND	PERP12	PERN12	GND	PERP13	PERN13
D	GND	PERP11	PERN11	GND	PERP10	PERN10

	7	8	9	10	11	12
A	GND	PETP14	PETN14	GND	PETP15	PETN15
B	GND	PETP9	PETN9	GND	PETP8	PETN8
C	GND	PERP14	PERN14	GND	PERP15	PERN15
D	GND	PERP9	PERN9	GND	PERP8	PERN8

	13	14	15	16	17	18
A	GND	FLEXIO1_RC	FLEXIO2_RC	GND	PETP0	PETN0
B	GND	RCLKp (Host out)	RCLKn (Host out)	GND	PETP7	PETN7
C	GND	FLEXIO1_NRC	FLEXIO2_NRC	GND	PERP0	PERN0
D	GND	RCLKp (Device in)	RCLKn (Device in)	GND	PERP7	PERN7

	19	20	21	22	23	24
A	GND	PETP1	PETN1	GND	PETP2	PETN2
B	GND	PETP6	PETN6	GND	PETP5	PETN5
C	GND	PERP1	PERN1	GND	PERP2	PERN2
D	GND	PERP6	PERN6	GND	PERP5	PERN5

	25	26	27	28	29	30
A	GND	PETP3	PETN3	GND	2WCL	2WDA
B	GND	PETP4	PETN4	GND	VCC12V	PRPE
C	GND	PERP3	PERN3	GND	VCC3P3V	PERST#
D	GND	PERP4	PERN4	GND	SCL	SDA

CN2 – USB Type-C Connector (SDB / SMART UART)

CN2 provides access to the Atlas3 debug and firmware-supported UART interfaces. When connected to a host computer, the USB interface exposes two COM ports:

USB Serial Interface	Function	Notes
COM Port 1	Atlas3 I²C slave interface	Requires managed firmware support
COM Port 2	Atlas3 SDB or SMART UART	Can be switched between SDB and SMART UART. SMART UART requires managed firmware support

The active path for the second interface can be selected using the **uart** CLI command.

CN3 – USB Type-C Connector (CLI)

CN3 connects directly to the onboard MCU and serves as the primary management interface for the host adapter. Use CN3 for CLI functions including:

- Board diagnostics and PCIe link monitoring
- Firmware updates
- Switch and CDFP configuration

When connected to a host computer, CN3 appears as a serial COM port. Connect to this port with a terminal emulator to access the MCU command prompt.

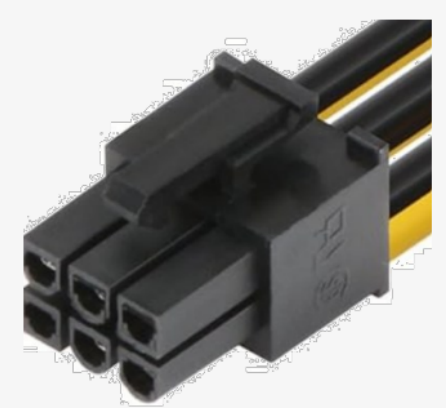
See **Command-Line Interface (CLI) Setup** for connection instructions and **CLI Command Reference** for supported commands.

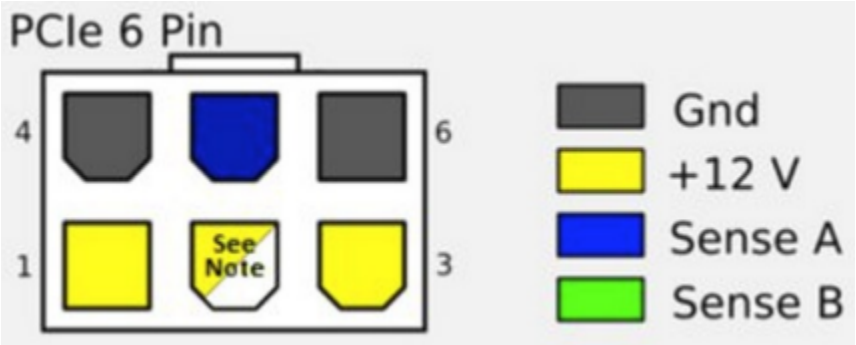
CN4 – 6-Pin 12 V Power Connector

CN4 provides the 12 V supply used by the CDFP interface. The connection routes additional 12 V power to pin **B29 (VCC12V)** of the CN1 CDFP connector.

This power path is separate from the host adapter's board-power requirement and is intended to support connected CDFP hardware that requires a 12 V supply, including compatible AOC or AEC cables.

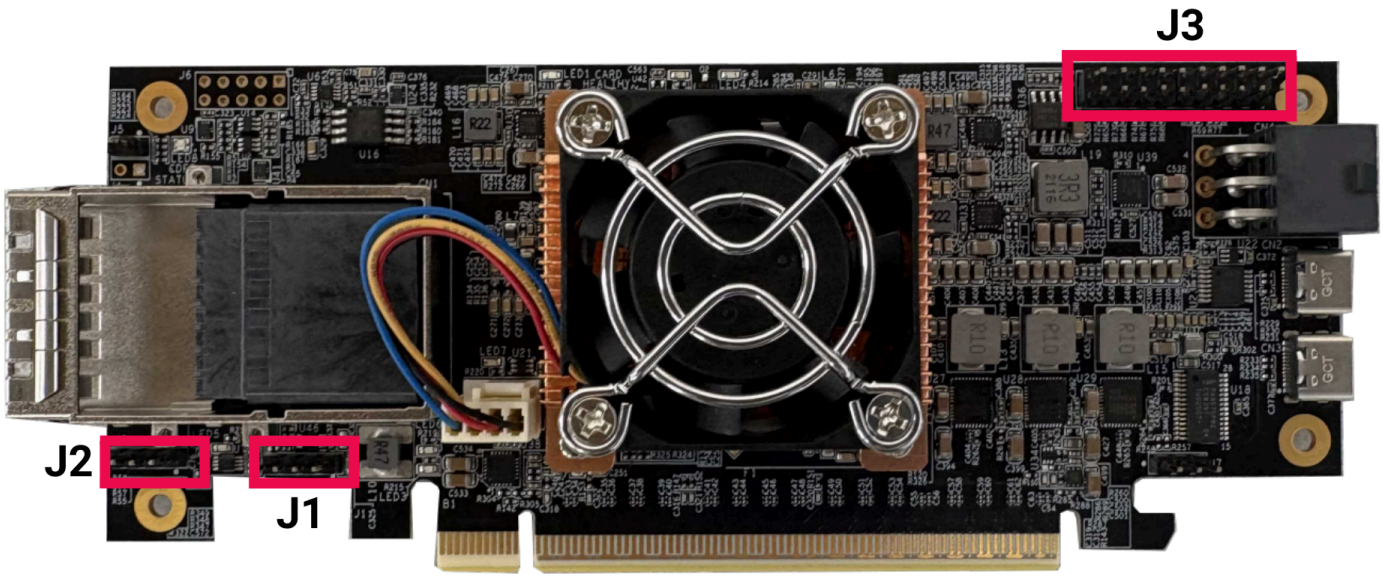
Pin	Signal
1	+12V
2	+12V
3	+12V
4	GND
5	SENSE A
6	GND





Internal Headers

The Atlas3 CDFP Host Adapter Card includes three onboard headers that provide direct access to UART, SDB, and low-level debug signals. Their locations are identified on the PCB.



J1 – SDB Header

J1 provides direct access to the Atlas3 SDB serial signals:

Pin	Signal
1	SDBTX
2	GND
3	SDB_RX
4	P1V8 (NC)

J2 – UART Header

J2 provides direct access to the UART transmit and receive signals:

Pin	Signal
1	UART_TX
2	GND
3	UART_RX
4	P1V8 (NC)

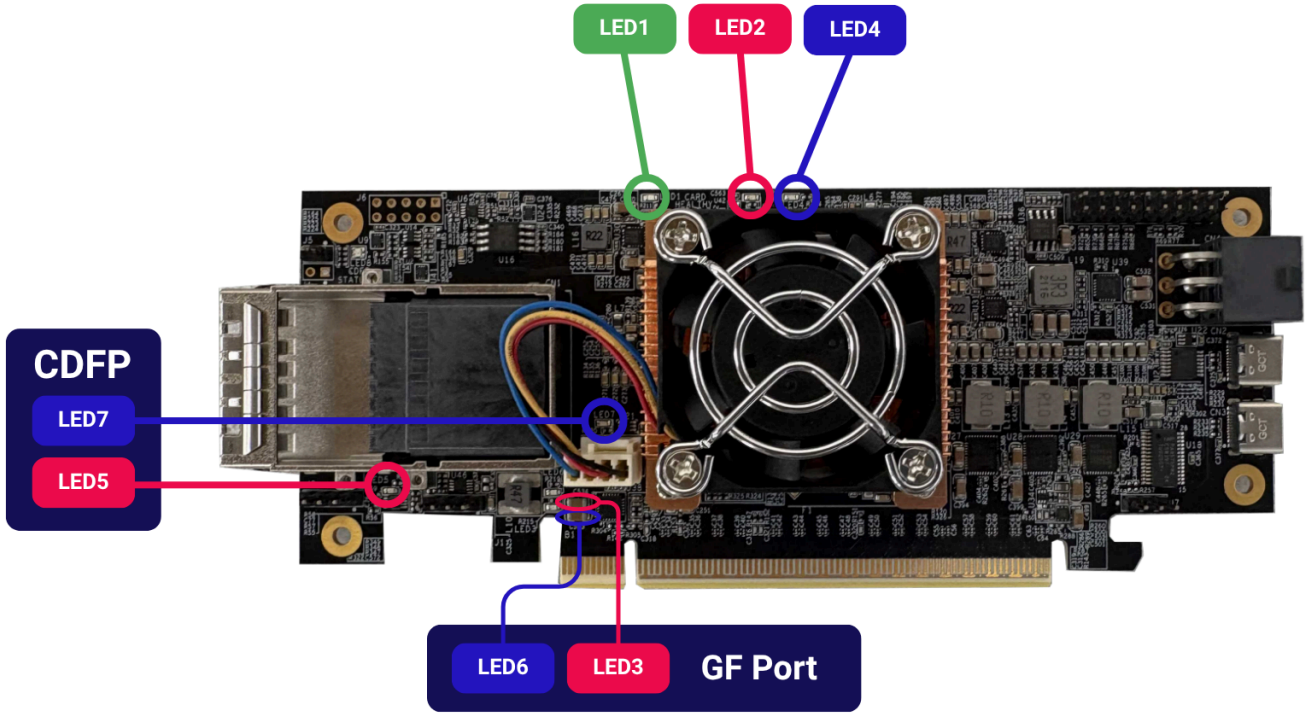
J3 – Debug Header

J3 is a 20-pin header that exposes Atlas3 debug, reset, and associated ground signals:

Even Pin	Signal	Odd Pin	Signal
2	NC	1	1.8V
4	GND	3	AVG_TRST_N
6	GND	5	AVG_TDI
8	GND	7	AVG_TMS
10	GND	9	AVG_TCK
12	GND	11	GND
14	GND	13	AVG_TDO
16	GND	15	SRST_N
18	GND	17	GND
20	GND	19	GND

LED Indicators

The Atlas3 CDFP Host Adapter Card includes status LEDs for monitoring switch operation, MCU activity, PCIe link speed, and link-width status.



System Status LEDs

LED ID	Color	Description
LED2	Red	**System Error Indicator.** Turns on for: • Second expiration of the watchdog timer • Built-In Self-Repair (BISR) error • Firmware signature authentication failure detected by IBR firmware • Double-bit ECC error during IBR reads • Other conditions classified by the switch as fatal
LED4	Blue	**Atlas3 Heartbeat.** Blinks when managed firmware is running normally. Remains solid on when unmanaged firmware is loaded.
LED1	Green	**MCU Status.** Blinks when the MCU firmware is active and responding.

Link Speed LEDs

The Link Speed LEDs (blue) indicate the negotiated PCIe generation for the host-side and CDFP links.

- **Active link** — The LED blink rate corresponds to the negotiated PCIe generation.
- **Gen6 link** — The corresponding LED remains solid.
- **Link down** — The LED remains off.
- **Detailed link status** — Use the **showport** CLI command to view negotiated speed and width.

LED ID	Location	Color
LED6	Golden finger	**Blue**
LED7	CDFP interface	**Blue**

Each LED blinks at a frequency proportional to the negotiated PCIe link speed:

PCIe Generation	Blink Rate
Gen1 (2.5 GHz)	0.25 Hz
Gen2 (5.0 GHz)	0.5 Hz
Gen3 (8.0 GHz)	1 Hz
Gen4 (16.0 GHz)	2 Hz
Gen5 (32.0 GHz)	4 Hz
Gen6 (64.0 GHz)	Solid (steady on)

- If no PCIe link is detected, the corresponding Link Speed LED remains off.

Link Width LEDs

The Link Width LEDs (red) provide a quick indication of lane-width status for the host-side and CDFP PCIe links.

LED ID	Monitored Port	Color
LED3	Golden finger	**Red**
LED5	CDFP interface	**Red**

Use the **showport** CLI command to compare the desired and negotiated link width for each interface and identify links reported as Active or Degraded.

- A **Degraded** status indicates that the negotiated link speed or width does not match the desired configuration.

Practical Applications and System Integration

The Atlas3 CDFP Host Adapter Card can extend a PCIe Gen6 x16 connection from a host system to compatible CDFP-equipped hardware. Supported configurations include:

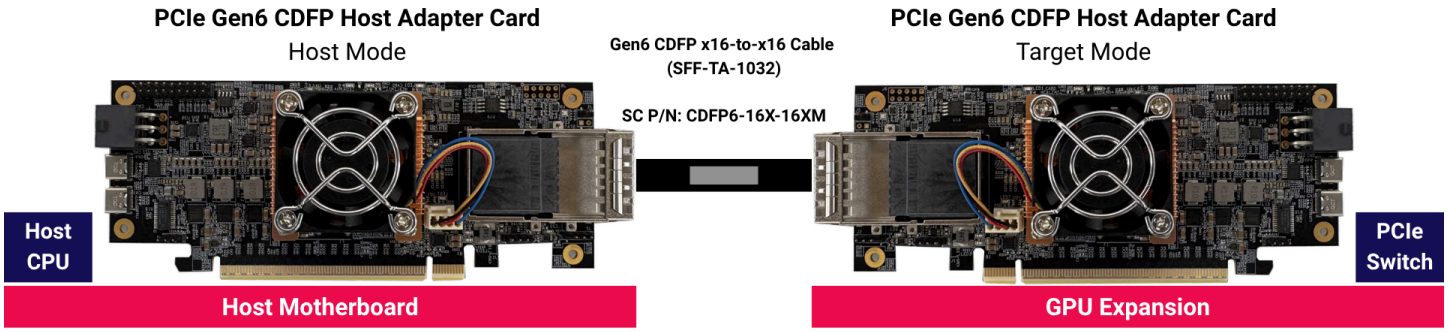
- **Host-to-target connection** — Connect directly to another Atlas3 CDFP Host Adapter Card.
- **CDFP adapter connection** — Connect to a compatible CDFP adapter for external PCIe hardware integration.

Host-to-Target CDFP Connection

Two Atlas3 CDFP Host Adapter Cards can be connected to create a host-to-target PCIe link. One card operates on the host side, while the second connects to the target expansion system.

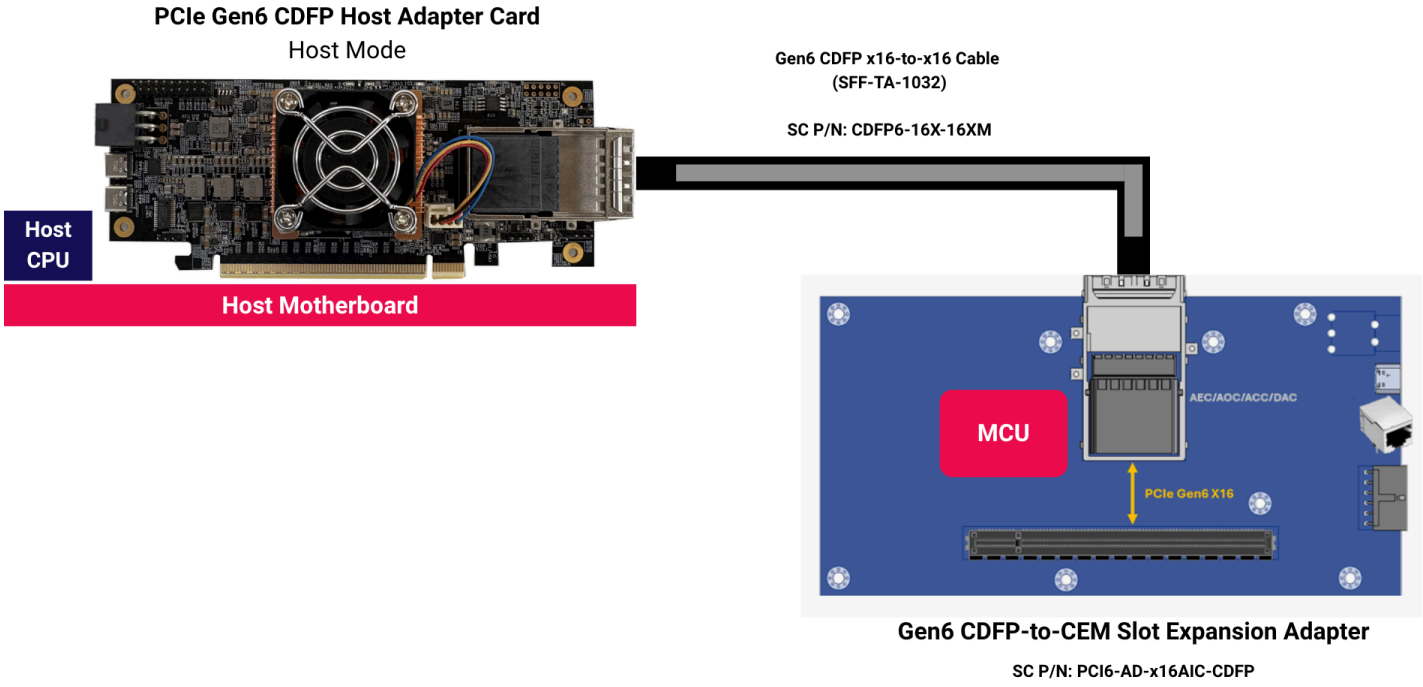
A **CDFP6-16X-16XM Gen6 cable (CDFP6-16X-16X-16XM)**, terminated with **SFF-TA-1032 CDFP x16 connectors at both ends**, connects the host-mode card to the target-mode card. The host-mode card is installed in the host motherboard, while the target-mode card is installed in a GPU expansion system containing the downstream PCIe switch.

Component	Description
Host Adapter	Atlas3 CDFP Host Adapter Card (this product), operating in host mode
Cabling	CDFP6-16X-16XM Gen6 CDFP x16 (SFF-TA-1032) to CDFP x16 cable
Target Adapter	Atlas3 CDFP Host Adapter Card (this product), operating in target mode
Target System	GPU expansion system with downstream PCIe switch



Connecting to the PCI6-AD-x16AIC-CDFP

The Atlas3 CDFP Host Adapter Card connects to the **PCI6-AD-x16AIC-CDFP** through a Gen6 CDFP x16 cable, extending the host's PCIe Gen6 x16 connection to an external **CEM x16 slot** for a compatible PCIe add-in card.



Command-Line Interface (CLI) Setup

The Atlas3 CDFP Host Adapter Card includes an onboard microcontroller (MCU) that provides command-line access for configuration, monitoring, diagnostics, and firmware management. The card includes two USB Type-C interfaces:

- **CN3 — Primary interface for MCU CLI access and firmware updates.**
- **CN2 — Provides Atlas3 SDB and SMART UART access and is not used for the standard MCU CLI.**

The CLI can be used to:

- Monitor temperature, critical voltages, fan speed, power consumption, and PCIe link status.
- Access switch and port registers for configuration and troubleshooting.
- Manage Atlas3 and MCU firmware updates.
- Control CDFP power, reset, and MUX signals and run board-level diagnostics.

Connection Steps

1. Connect a USB Type-C cable between the host computer and the **CN3** connector on the Atlas3 CDFP Host Adapter Card.

2. After the USB connection is detected, identify the assigned COM port using your system's Device Manager.

3. Open your serial terminal software (Tera Term, PuTTY, or equivalent) and connect to the assigned COM port.

4. A successful serial connection displays the MCU command prompt.

CLI Command Reference

Commands	Description
help	Display all available commands
fdl	Upgrades Atlas3 unmanaged or managed firmware and onboard MCU firmware
lsd	Displays system telemetry, including temperature, critical voltages, fan speeds, and board power consumption
mw	Writes a 32-bit value to a specified register within the Atlas3 switch
dr	Dumps all switch-level registers for diagnostic or debugging purposes
dp	Dumps port-specific switch registers for the selected port
df	Dumps contents of the switch's onboard flash memory
showport	Displays link status and connection details for USP/DSP ports
bist	Runs the onboard Built-In Self-Test (BIST) for device diagnostics
setmode	Set clock mode of host card
showmode	Displays the current clock mode of the host card
spread	Configures the PCIe clock spread spectrum setting
clk	Enables or disables the PCIe clock output
sdb	Sets the MCU SDB port state (on/off)
uart	Selects the CN2 UART path between SMART UART and the Atlas3 SDB interface
pwr	Displays the status of the onboard power regulators
cdfp	Displays and controls CDFP power, reset, and MUX signals
counters	Displays error counters and statistics for all active ports
ver	Displays version information for the host card, MCU firmware, and Atlas3 firmware
sysinfo	Performs reset functions for the onboard MCU, PCIe hierarchy, or Atlas3 switch
reset	Performs a soft reset of the onboard MCU

Command Usage Notes

Firmware Upgrade and Management – fdl

The **fdl** command is used to upgrade the Atlas3 firmware, including unmanaged switch firmware, managed firmware, and MCU firmware. Firmware is transferred over the serial interface using the XMODEM protocol.

Enter the command **fdl** followed by the target upgrade mode. There are four to choose from:

- **mini** – Updates the unmanaged mini SBR firmware.
- **main** – Updates the unmanaged main SBR firmware.
- **fw** – Updates the managed switch firmware.
- **mcu** – Updates the on-board MCU firmware.

When executed, the system prompts for confirmation before erasing and writing flash memory.
Press **Y** to continue or **Ctrl+X** to cancel.

The **mini**, **main**, and **fw** commands erase the Atlas3 switch flash before the new firmware is written.
Firmware data is transferred using the XMODEM protocol from the host system.

Firmware Upload Procedure

Step 1 – Connect via Serial Interface

- Connect a USB-C cable to the host card's **CN3** port.
- Identify the COM port in your system's **Device Manager**.
- Open a terminal emulator such as **TeraTerm/puTTy** (Windows) or **minicom** (Linux) and connect to that COM port.
- A successful connection will display the command prompt (Cmd>).

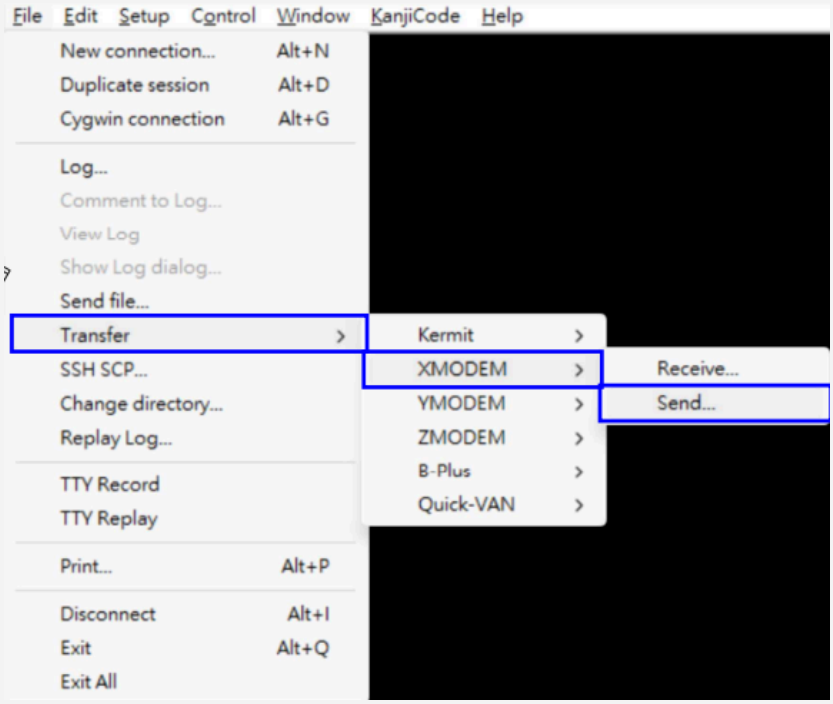
Step 2 – Run the Upload Command

1. Enter the appropriate **fdl** command (e.g., **fdl main**).
2. When prompted, press **Y** to confirm the upgrade or **Ctrl+X** to cancel.
3. The flash memory will be erased, and the system will wait for incoming data via XMODEM.

Continued on the next page.

Step 3 – Send the Firmware File via XMODEM

- In **TeraTerm** – Go to **File** → **Transfer** → **XMODEM** → **Send**, then select the **BIN firmware file**.



- In **minicom** – Use **Send File** → **XMODEM** and choose the **BIN firmware file**.

Step 4 – Apply the New Firmware

- After the upload finishes, power cycle the host card for unmanaged or managed firmware updates. For MCU firmware upgrades, use the **reset** command instead of a power cycle to activate the new MCU firmware.

System Diagnostics (Sensors and Power) – lsd

The **lsd** command displays real-time system diagnostics for the Atlas3 CDFP Host Adapter Card, including temperature, fan speed, voltage readings, and power consumption. This information helps monitor board health, identify abnormal conditions, and verify proper cooling and power delivery.

The output includes:

- **Thermal** – Reports the temperature near the Atlas3 PCIe switch.
- **Fan Speed** – Shows the host card fan RPM.
- **Voltage Sensors** – Reports monitored onboard rails, including **P1V8_IN**, **P1V5_IN**, **P1V2_IN**, **P0V85_IN**, and the monitored 0.8 V rails.
- **Power Consumption** – Reports voltage, current, and power readings for the host-card (**P12VGF_IN**) and CDFP (**P12CDFP_IN**) 12 V inputs.

Register Write – mw

The **mw** command writes a 32-bit value to a specific register address within the Atlas3 PCIe switch. It writes the specified hexadecimal data directly to the target register for switch configuration and low-level hardware control.

Enter the command **mw** followed by the register address (hex) and the data value (hex) to be written. Valid register addresses range from **0x00000000** to **0xFFFFFFFC**, and writable data values range from **0x00000000** to **0xFFFFFFFF**. For example:

- **mw fff0017c ffffffff** – This writes the data **0xFFFFFFFF** to the register address **0xFFF0017C** on the Atlas3 switch

Switch Register Dump – dr

The **dr** command reads and dumps switch-wide register values from the Atlas3 PCIe switch.
It retrieves low-level register data across the switch's address space for debugging, validation, and hardware bring-up.

Enter the command **dr** followed by the starting register address (hex) and an optional count (hex) to specify how many bytes to read. The valid register addresses and count values range from **0x00000000** to **0xFFFFFFFC**. For example:

- **dr 60800000** – Dumps the values in Atlas3 switch registers starting from address 0x60800000.

Register Address Mapping

Each port's register block is separated by an offset of 0x8000. The following base addresses apply to the active PCIe interfaces on this card:

Interface	Port	Base Address
CDFP x16 connector	0	0x60800000
Golden finger	32	0x60900000

Port Register Dump – dp

The **dp** command reads and dumps port-specific register values from the Atlas3 PCIe switch.
It displays low-level hardware data for a selected physical port and is primarily used for port-level debugging and validation.

Enter the command **dp** followed by the port number (0–47) to dump switch registers for that port. For example:

- **dp 32** – Dumps switch register values for Port 32.

Flash Dump — df

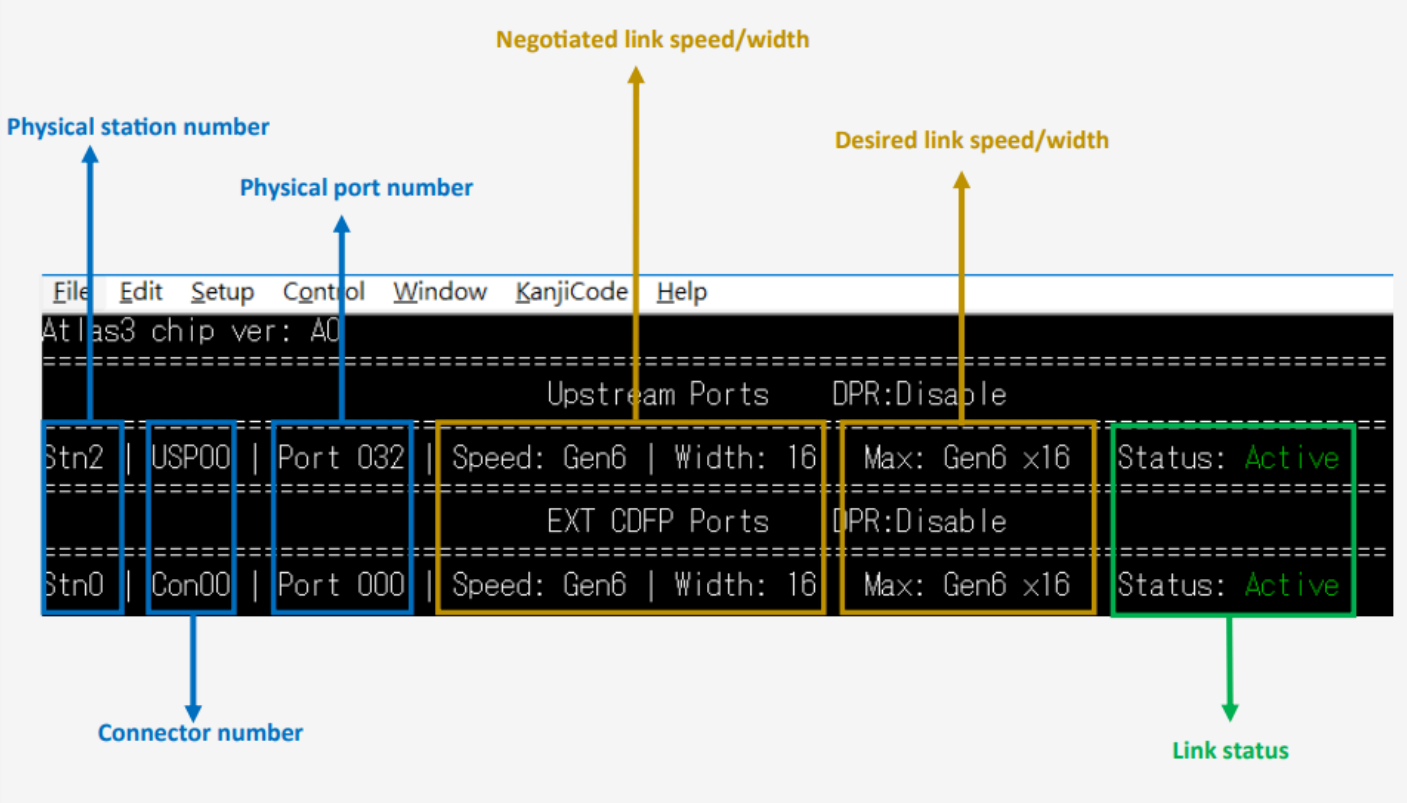
The **df** command reads and dumps the contents of the switch flash memory to the console or a connected host interface. It retrieves raw flash data for firmware inspection, debugging, or verification.

Enter the command **df** followed by the start address (hex) and optionally the byte count (hex) to dump data from the switch flash memory. Both the address and count can range from 0x00000000 to 0xFFFFFFFC. For example:

- **df 400** – Dumps the flash contents starting from address 0x00000400
- **df 400 4** – Dumps 4 bytes of flash data starting from address 0x00000400.

Port Link Status— showport

The **showport** command displays the link status for all upstream (USP) and downstream (DSP) ports on the Atlas3 PCIe switch. The output shows each port's station number, connector or upstream-port identifier, physical port number, negotiated link speed and width, desired link speed and width, and current link status:



Output Field Descriptions

Field	Description
Station Number (Stn)	Physical station index on the Atlas3 switch.
Connector / Port ID	Identifies the CDFP connector or upstream PCIe interface.
Physical Port Number (Port)	Physical switch port number assigned to the interface.
Speed	The **negotiated PCIe generation** (e.g., Gen1, Gen4, Gen6).
Width	The **negotiated link width** (e.g., x1, x4, x8, x16).
Max	The **desired PCIe link** speed and width for the port.
Status	Current link condition (Active, Idle, or Degraded).

Status Definitions

- **Degraded** – Link trained successfully but negotiated speed or width is lower than expected.
- **Idle** – No physical link detected or device not present on the port.
- **Active** – Desired and negotiated link speed/width matched successfully.

Built-In Self-Test — bist

The **bist** command runs a basic diagnostic routine on the Atlas3 CDFP Host Adapter Card. It checks communication with onboard I²C devices and reports the status of each detected component.

The diagnostic covers devices such as power regulators, EEPROM, I²C I/O expanders, I²C multiplexers, clock generators, and clock buffers.

The test runs automatically once invoked and reports **OK** or **FAIL** results for each test item:

Channel	Device	Address	Status
CH0	PCA9575-0	0x40	OK
CH0	PCA9575-1	0x42	OK
CH0	PCA9551PW	0x4C0	OK
CH0	MP2971	0xBE	Fail
CH0	AT24C16	0xA0	OK
CH0	RC21012	0x12	OK

Host Card Mode Configuration — setmode

The **setmode** command selects the PCIe reference-clock mode used by the Atlas3 switch. It determines whether the switch uses the reference clock supplied through the PCIe golden-finger edge connector or a clock generated locally on the host card.

Enter the command **setmode** followed by the mode number (1–2) to configure the host card's operating mode.

Mode	Description
1 – Buffer mode	The Atlas3 system reference clock uses the same clock domain as the reference clock supplied through the PCIe golden-finger edge connector.
2 – Generator mode	The Atlas3 system reference clock is sourced from the card's local clock generator.

Show Host Card Mode — showmode

The **showmode** command displays the current PCIe reference-clock mode of the Atlas3 CDFP Host Adapter Card. Use it to confirm whether the card is operating in Buffer mode or Generator mode after running **setmode**.

PCIe Clock Spread Setting — spread

The **spread** command configures spread-spectrum behavior for the Atlas3 PCIe reference clock. It can operate with spread disabled or with down-spreading of 3,000 ppm or 5,000 ppm.

Enter the command **spread** followed by the **1**, **2**, or **off**:

Command	Clock Behavior
spread 1	3,000 ppm down-spread (-0.3%)
spread 2	5,000 ppm down-spread (-0.5%)
spread off	Spread spectrum disabled

PCIe Clock Output Control – clk

The **clk** command controls whether the host card outputs a PCIe reference clock through the CDFP connector to attached hardware. This reference clock provides the timing source used by the connected PCIe device for link initialization and operation. Disabling the output removes the reference clock from the CDFP interface without disabling the Atlas3 switch's own system reference clock.

This allows engineers to control downstream clock delivery independently when bringing up or troubleshooting a CDFP connection.

- **clk en** – Enables PCIe clock output to the CDFP interface
- **clk dis** – Disables PCIe clock output to the CDFP interface

Clock Output Guidelines

- Clock output can be changed dynamically and does not require a host card power cycle.
- The setting is stored in the MCU and applied automatically the next time the host card powers on.
- The Atlas3 switch system reference clock remains enabled regardless of the CDFP clock-output setting.

SDB Port Control — sdb

The **sdb** command enables or disables the Atlas3 Serial Debug Bridge (SDB) interface. It determines whether the board remains in normal MCU-controlled CLI operation or makes the SDB interface available for external Broadcom debug utilities.

Enter the command **sdb** followed by **off** or **on**:

Command	Description	Typical Use
sdb on	Sets the MCU SDB state to ON.	Used for **normal operation** like running CLI commands such as **fdl**, **mw**, **dr**, **dp**, and **showport**.
sdb off	Sets the MCU SDB state to OFF.	Used for **utility mode** – running host-based tools such as **SwitchCLID** or **ARCTIC** from a PC.

SDB Behavior Notes

- Only one mode is active at a time (normal MCU/CLI operation or SDB utility access).
- Setting **sdb off** switches the board from normal MCU/CLI operation to SDB access for host-based utilities.

Utilities such as SwitchCLID and ARCTIC are Broadcom-provided tools distributed under NDA and SLA. Contact Broadcom for licensing, access, or additional support information.

UART Path Selection — uart

The **uart** command selects the UART path for the CN2 (USB Type-C) interface, switching between the Atlas3 SDB (Serial Debug) interface and the SMART UART interface.

Enter the command **uart** followed by **0** or **1**:

- **uart 0** – Routes CN2 to SMART UART
- **uart 1** – Routes CN2 to SDB (default)

UART Path Notes

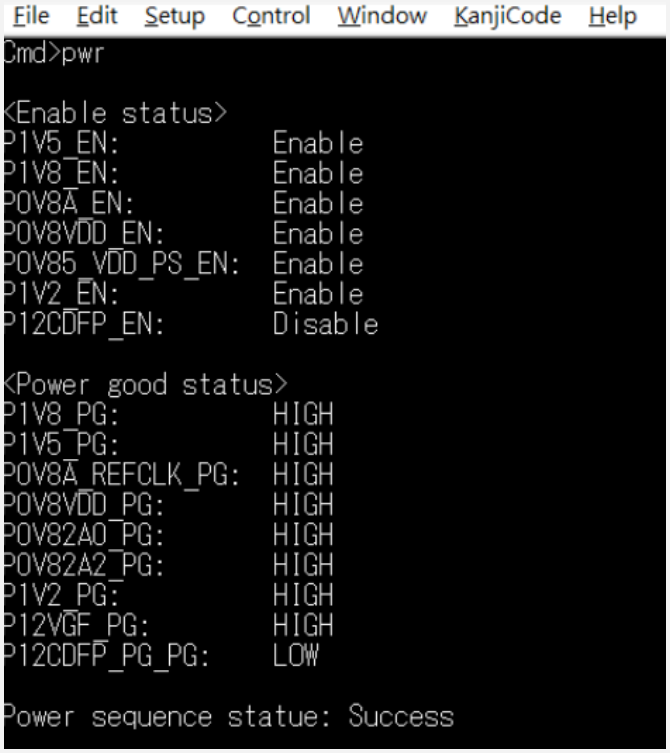
- The selected UART path is stored and applied after a power cycle.
- SDB (Serial Debug) is supported in both managed and unmanaged firmware modes.
- SMART UART is supported only in managed firmware mode.

Power Status — pwr

The **pwr** command displays the current power status of the Atlas3 CDFP Host Adapter Card, including power-rail enable states, power-good signals, and overall power sequencing status. A “Success” power sequence status indicates all required rails initialized correctly.

The output is organized into:

- **Enable Status** — Shows whether each monitored power rail is enabled or disabled.
- **Power-Good Status** — Reports the power-good state for each monitored rail.
- **Power Sequence Status** — Reports whether the board power-up sequence completed successfully.



CDFP Control and Status — cdfp

The **cdfp** command displays and controls power, reset, and MUX signals for the CDFP interface.

Enter **cdfp** by itself to view the current CDFP status, or specify a target and action to change an individual signal.

Target	Supported Actions	Function
p12v	**en** , **dis**	Enables or disables the CDFP 12 V power supply.
perst	**1**, **0**, **high**, **low**	Sets the CDFP PERST# signal high or low.
mux0	**1**, **0**, **high**, **low**	Sets the CDFP **MUXSEL_0** signal high or low.
mux1	**1**, **0**, **high**, **low**	Sets the CDFP **MUXSEL_1** signal high or low.

For example:

- **cdfp** – Displays the current status of the CDFP signals.
- **cdfp p12v en** – Enables 12 V power to the CDFP interface.
- **cdfp perst 1** – Sets the CDFP PERST# signal high.
- **cdfp perst 0** – Sets the CDFP PERST# signal low.
- **cdfp mux0 1** – Sets MUXSEL_0 high.
- **cdfp mux1 0** – Sets MUXSEL_1 low.

Port Error Counters — counters

The **counters** command displays error counters for each active port on the Atlas3 PCIe switch. The output includes **PortRx**, **BadTLP**, **BadDLLP**, **RecDiag**, **LinkDown**, and **FlitError** counters, providing a quick view of link and protocol-level errors across the switch.

- **counters** – Displays the current error counts for all ports.
- **counters clear** – Resets all port error counters to zero.

About Error Counter Behavior

- The FLIT error counter increments by 1 when enabled and a countable event occurs, as defined by the FLIT Error Counter Control Register.
- If non-zero, the counter decrements at a fixed rate based on the link encoding and width.
- The counter is cleared when the FLIT Error Counter Enable bit transitions from **0b** to **1b**.

System Version — ver

The **ver** command displays host card identification and version information for the MCU and Atlas3 switch. Use it to verify the running firmware and switch mode before or after a firmware update.

---------- Product Info ----------	
Company :	Serial Cables
Model :	PCI6_AD_x16HE_CDFP_BG6
Serial No. :	
---------- App Info ----------	
Version :	0.0.1
Build Time :	Aug 5 2026 19:52:38
---------- SBR Info ----------	
Version:	0022A006
Switch Mode:	Unmanaged mode

System Information — sysinfo

Displays a complete summary of the Atlas3 CDFP Host Adapter Card's configuration and operating status, including firmware information, board telemetry, power status, PCIe link state, CDFP status, clock configuration, and onboard device diagnostics.

This is effectively a sequence of several key commands (**ver**, **lsd**, **clk**, **pwr**, **showport**, **cdfp**, **showmode**, **bist**), consolidated into a single report for quick system validation.

System Reset — reset

The **reset** command provides several reset functions for the Atlas3 CDFP Host Adapter Card. It can reset the onboard MCU, reset a PCIe hierarchy through its PERST# signal, or send a system power-on reset to the Atlas3 switch.

Enter the command **reset** followed by an optional reset type to control how the host card is reset. For example:

- **reset** – Reset the onboard MCU.
- **reset s0** – Resets the S0 PCIe hierarchy through **S0_PCE_PERST_N**
- **reset s1** – Resets the S0 PCIe hierarchy through **S1_PCE_PERST_N**
- **reset sw** – Sends a system power-on reset (**SYS_PWR_ON_RST_N**) to the Atlas3 PCIe switch.

The **reset** command can also be used after an MCU firmware update to activate the new firmware without power cycling the host card.

Maintenance & Diagnostics

The Atlas3 CDFP Host Adapter Card includes CLI commands and onboard indicators for checking board health, PCIe link status, power delivery, and CDFP operation. The following checks can help isolate common issues during bring-up, testing, or troubleshooting.

- **For a general system check**, run **sysinfo** to collect firmware information, board telemetry, power status, PCIe link state, CDFP status, clock configuration, and onboard device diagnostics in a single report.

- **If a PCIe link does not train as expected**, run **showport** to compare the negotiated and desired link speed and width. A **Degraded** status indicates that the negotiated speed or width does not match the desired configuration. Use **counters** to check for accumulated port errors.

- **If a power issue is suspected**, run **pwr** to check power-rail enable, power-good, and sequencing status. Use lsd to review voltage readings and power consumption, and **cdfp** to confirm the current CDFP 12 V power state.

- **If the Atlas3 System Error LED (LED2) is illuminated**, run **bist** to check communication with onboard I²C devices and **lsd** to review temperature, voltage, fan speed, and power telemetry.

- **After a firmware update**, run **ver** to confirm the installed MCU and Atlas3 firmware versions. Atlas3 managed or unmanaged firmware updates require a host-card power cycle, while an MCU firmware update can be applied using the **reset** command.

Revision History

Revision	Description
1.2	Reformatted and restyled for brand consistency and readability. Rewritten for clarity. Added *Product Overview*, *Safety, Handling & Compliance*, *Maintenance & Diagnostics,* and *Contact Us* sections.
1.1	Updated cover and disclaimers.
1.0	Initial manual release.

Contact Us

For technical assistance, product inquiries, or additional documentation, our team is here to help.

Support

📧 **support@serialcables.com**

Sales

📧 **sales@serialcables.com**

Phone

📞 **+1 (303) 495-2320**

Website

🌐 **https://serialcables.com/**