Hermes | PCIe 6.0 x16 and X8 EDSFF AIC Redriver Card

TECHNICAL MANUAL

Revision 1.3 July 2026

PPCI6-AD-x16EDSFF-E3-H-SC / QA
PPCI6-AD-x8EDSFF-E3-H-SC / QA

Modular Paddle Cards

PCI EXPRESS 6.0

USB Type-C CLI Interface

CXL Compute Express Link™

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Declaration and Revision Notice

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Product Overview

The GEN6 EDSFF Redriver Board is a linear signal conditioning adapter for PCIe® Gen6 and CXL™ links operating at 64 GT/s. Built around Phison PS7161 redriver ICs, it improves signal integrity across high-loss channels without altering PCIe or CXL protocol behavior.

The board compensates for signal loss caused by long PCB traces, connectors, backplanes, and cable assemblies by applying configurable receiver equalization, flat gain, and transmitter swing on a per-lane basis. This helps extend reach, improve channel margin, and stabilize link training in demanding Gen6 environments.

Implemented as an add-in card (AIC), the GEN6 Redriver Board is commonly used in signal-integrity validation, interoperability testing, compliance preparation, and early system bring-up for PCIe Gen6 and CXL devices. Its linear architecture preserves transparent forwarding, allowing engineers to evaluate link behavior without protocol interference.

Key Features

- **PCIe Gen6 / CXL Support** – Designed for 64 GT/s signaling with support for NVMe and CXL traffic.
- **Phison PS7161 Redriver ICs** – Uses PS7161 linear redriver ICs with per-lane receiver equalization, flat gain, and transmitter swing control to correct channel loss.
- **Extended Reach –** Compensates for insertion loss from connectors, cables, backplanes, and long trace paths.
- **Protocol-Agnostic Operation** – Transparent forwarding suitable for link characterization and interoperability testing.
- **Adjustable EQ / Gain** – EQ, gain, and swing can be adjusted per chip or globally through the MCU CLI.
- **AIC Form Factor** – Add-in card design that drops easily into host systems, lab rigs, and test platforms.
- **Built-In Monitoring and Diagnostics** – Includes temperature and current readings, device detection, and BIST.
- **QA Options** – Optional Quarch PAM mezzanine support.

Safety, Handling, and Compliance

The PCIe Gen6 Redriver Board is intended for use in professional lab, validation, and system-integration environments. Follow all safety and handling guidelines to protect the board, connected systems, and high-speed components during operation or servicing.

Electrical Safety

- Always remove system power before installing or removing the redriver board or adjusting DIP switch settings.
- Do not touch exposed power pins or signal pads while the board is energized.
- Use a properly grounded DC power source and ensure the host system maintains chassis earth grounding.
- Never operate the board with damaged cables, connectors, or power leads.

ESD Protection

- Handle the board only in an ESD-controlled workspace.
- Use a grounded wrist strap and avoid contact with connector pads, component pins, or differential lanes.
- Keep the board in anti-static packaging when not in service or transport.
- High-speed redriver ICs are sensitive to static discharge. Improper handling may cause immediate or latent failure.

Thermal and Airflow Considerations

- Ensure adequate airflow across the board when operating at Gen6 speeds; redriver ICs may reach elevated temperatures under continuous load.
- Install the board in a chassis or bench setup that does not obstruct airflow around the components.
- Operate the board only within its specified ambient temperature range (0 °C to +40 °C typical).
- Persistent overheating may degrade signal integrity or trigger link-training instability.

Compliance

This product is manufactured in accordance with standard international safety and environmental regulations:

- **CE** – Conforms to applicable European EMC and low-voltage directives.
- **FCC Class A** – Intended for use in commercial or industrial environments.
- **RoHS 3** – Compliant with the Restriction of Hazardous Substances directive.

Hardware Overview

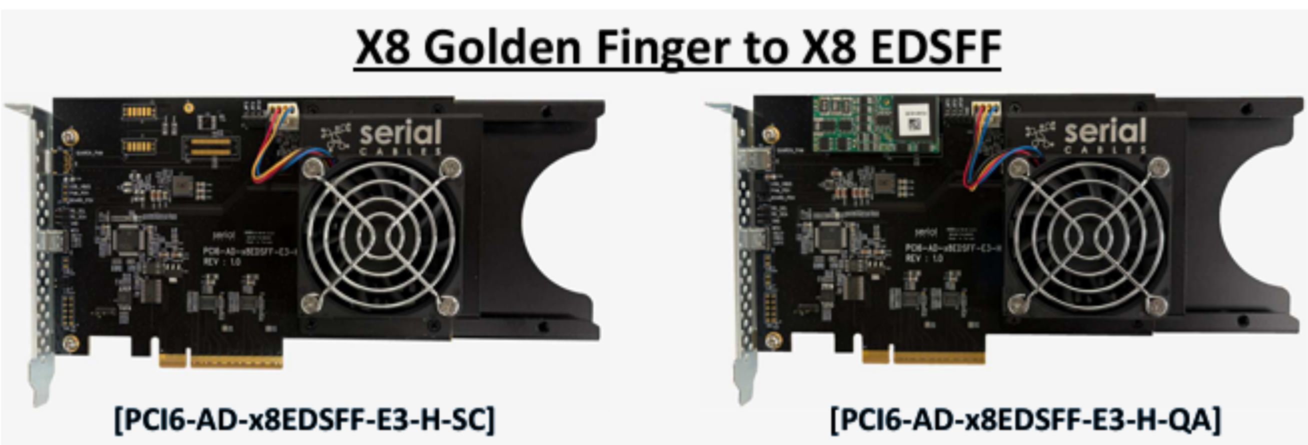
The PCIe Gen6 Redriver Board integrates high-speed linear redriver ICs, an EDSFF device interface, power and control headers, and lane-mapping optimized for EDSFF-based PCIe/CXL applications. The board provides a clean mid-channel signal path for host-to-device and device-to-host links while allowing users to configure power routing and control signals as required.

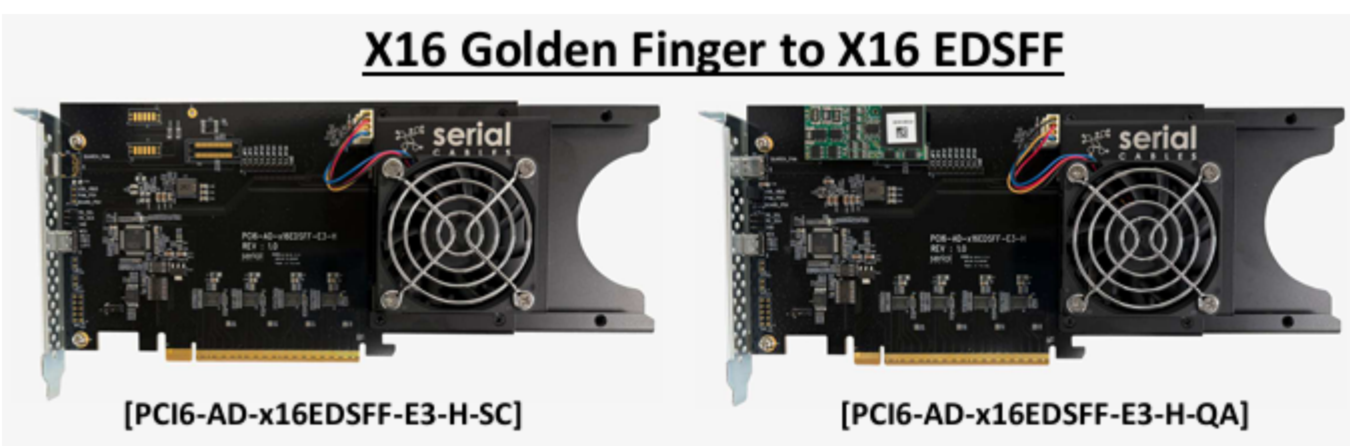
Form Factor

The redriver is implemented as a **PCIe add-in card (AIC)**, using a standard **PCIe golden-finger connector** on the host side and an **EDSFF interface** on the device side. The golden finger plugs directly into a PCIe x8 or x16 host slot, allowing the card to sit inline between the host and an attached EDSFF SSD or test device.

High-speed signals pass through the onboard redriver before reaching the EDSFF connector, enabling linear signal conditioning and tuning without altering the host or device.

- **SC variant**: Standard configuration for signal tuning, bring-up, and general bench validation.
- **QA variant**: Adds hardware support for automated validation and power analysis, including Quarch PAM mezzanine connectivity.





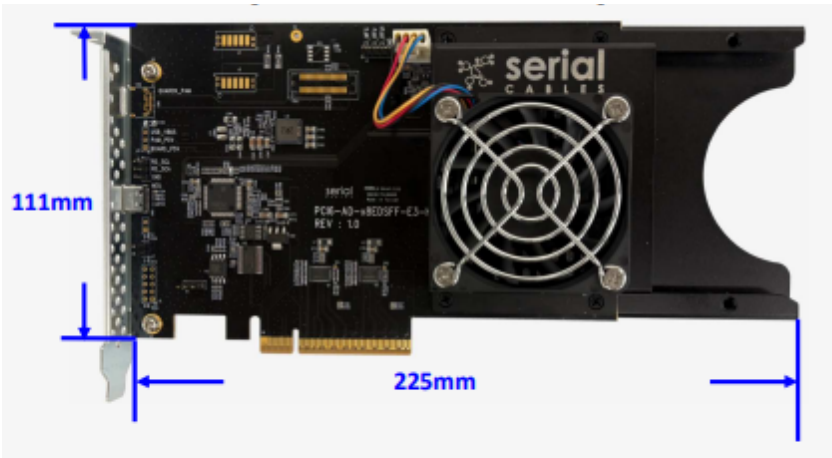
Board Dimensions

The adapter is offered in two EDSFF configurations:

Part Number	Lane Configuration	Length	Height
PG6-AD-x8EDSFF-E3-H-SC	x8	225 mm	111mm
PG6-AD-x16EDSFF-E3-H-SC	x16	255 mm	111mm
PG6-AD-x8EDSFF-E3-H-QA	x8	225 mm	111mm
PG6-AD-x16EDSFF-E3-H-QA	x16	255 mm	111mm

Both variants use the same PCB height and cooling module assembly.

x8

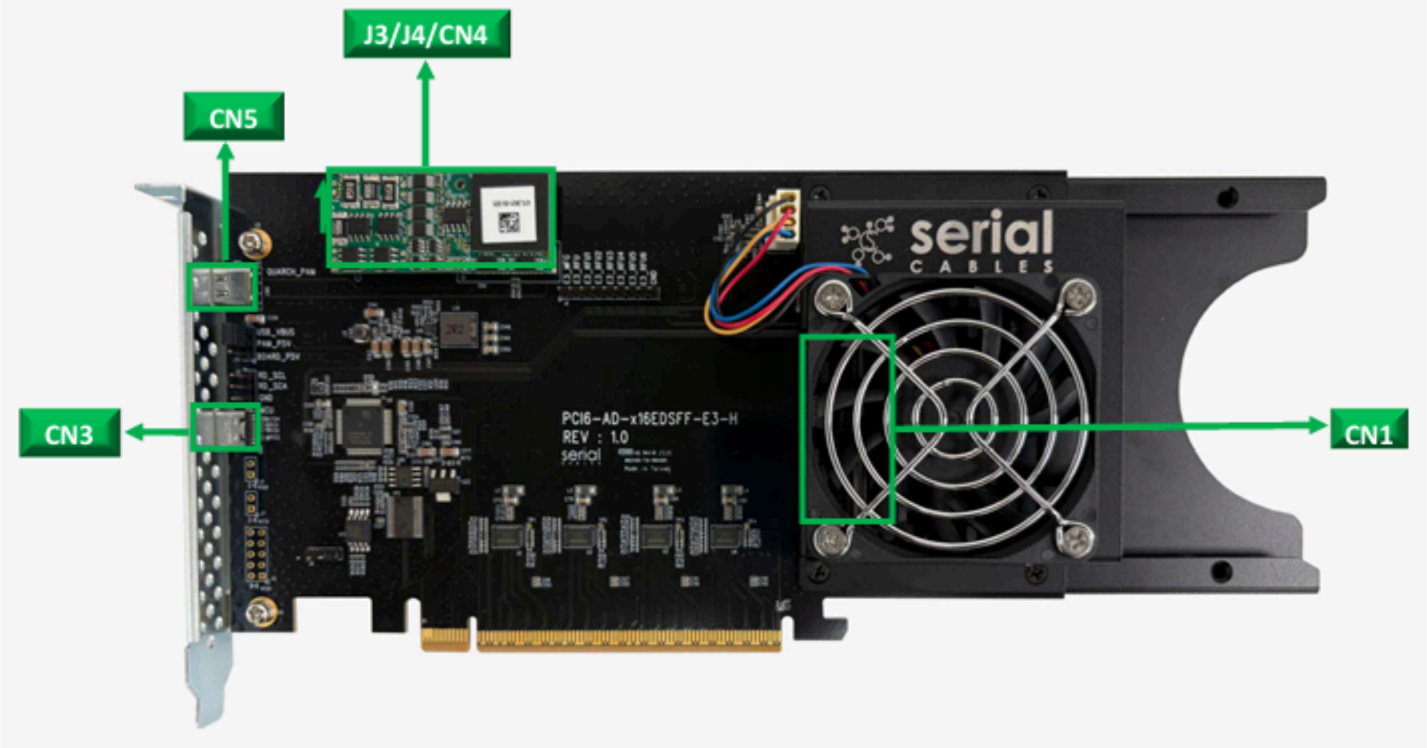


x16

Connector Overview

The PCIe Gen6 Redriver Board includes multiple connectors to support EDSFF device attachment, power delivery, management, and test automation. Connector population varies by board variant.

Connector	Description
J3 / J4 / CN4	Connectors for Quarch PAM Mezzanine modules
CN5	USB Type-C connector used to interface with Quarch Power Studio for power measurement and control.
The above connectors are populated on PCIG-AD-x8EDSFF-E3-H-QA and PCIG-AD-x16EDSFF-E3-H-QA variants only.	
CN1	Straddle EDSFF connector for high-speed PCIe/CXL signaling: ● x8 (84-pin) for PCIG-AD-x8EDSFF-E3-H-SC / QA ● x16 (140-pin) for PCIG-AD-x16EDSFF-E3-H-SC / QA
CN3	USB Type-C connector providing MCU access for CLI commands, redriver EQ configuration, and EDSFF side-band signal control.



Header Functions

The PCIe Gen6 Redriver Board includes several onboard headers used for power selection, management communication, and manufacturing or validation checks. Header population and usage depend on the board variant.

J10 – PAM_P5V Power Source Selection

J10 selects the source of the **PAM_P5V** supply rail used by auxiliary modules.

Jumper Position	Function
Pins 1-2	PAM_P5V sourced from **USB connector**
Pins 2-3	PAM_P5V sourced from **on-board power regulator**

Pin	Signal
1	P5V
2	PAM_P5V
3	USB_VBUS

Populated on PCIG-AD-x8EDSFF-E3-H-QA and PCIG-AD-x16EDSFF-E3-H-QA variants only.

J9 – Redriver I²C / SMBus Interface

J9 provides I²C/SMBus access to all redriver ICs on the board. This header is typically used for configuration, monitoring, or debug during bring-up and validation.

Pin	Signal
1	GND
2	RD_SDA
3	RD_SCL

J6 – Manufacturing (MFG) and FRU Signal Header

J6 exposes manufacturing and FRU-related signals for level checking and validation. Signal mapping differs between x8 and x16 board variants.

PCIG-AD-x8EDSFF-E3-H-SC / QA		
Pin in Header	**Signal**	**Pin in EDSFF**
1	EDSFF_MFG	EDSFF_B7
2	EDSFF_FRU	EDSFF_B8
3	EDSFF_FRU1	EDSFF_A42
4	GND	—

PCIG-AD-x16EDSFF-E3-H-SC / QA		
Pin in Header	**Signal**	**Pin in EDSFF**
1	EDSFF_MFG	EDSFF_B7
2	EDSFF_FRU	EDSFF_B8
3	EDSFF_FRU1	EDSFF_A42
4	EDSFF_FRU2	EDSFF_A68
5	EDSFF_FRU3	EDSFF_A69
6	EDSFF_FRU4	EDSFF_A70
7	EDSFF_FRU5	EDSFF_B68
8	EDSFF_FRU6	EDSFF_B69
9	GND	—

Redriver IC Locations

This section illustrates the physical placement of the redriver ICs and the relative trace lengths between the host interface and the EDSFF connector.

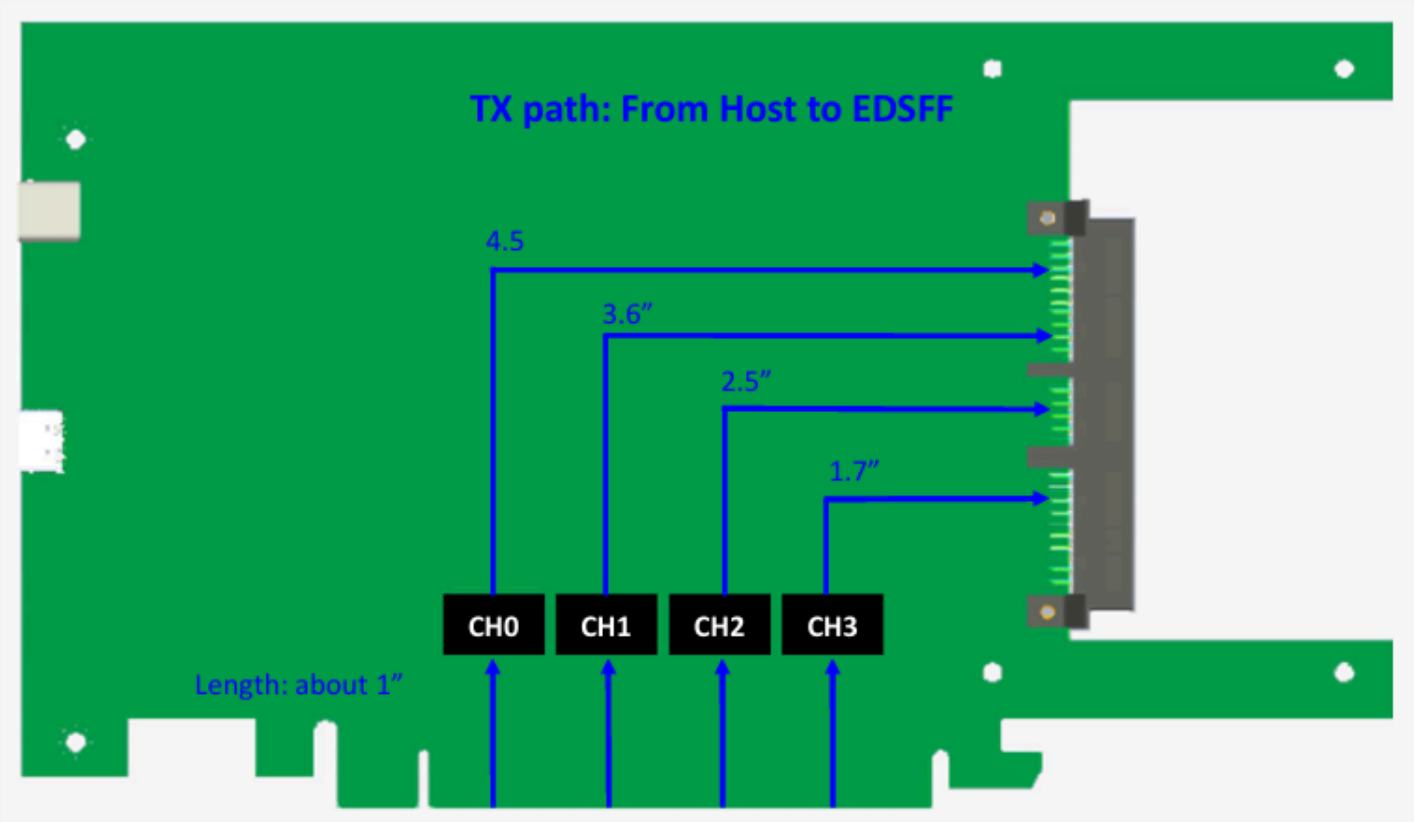
Separate diagrams are provided for transmit (TX) and receive (RX) paths to reflect direction-specific routing and signal-conditioning requirements. Trace length references are shown to support signal integrity analysis and validation.

PCIG-AD-x16EDSFF-E3-H-SC / QA

TX Path – From Host to EDSFF

Channels CH0 through CH3 are routed through individual redriver ICs, with progressively shorter trace lengths toward the connector.

- **CH0** – 4.5 inches
- **CH1** – 3.6 inches
- **CH2** – 2.5 inches
- **CH3** – 1.7 inches

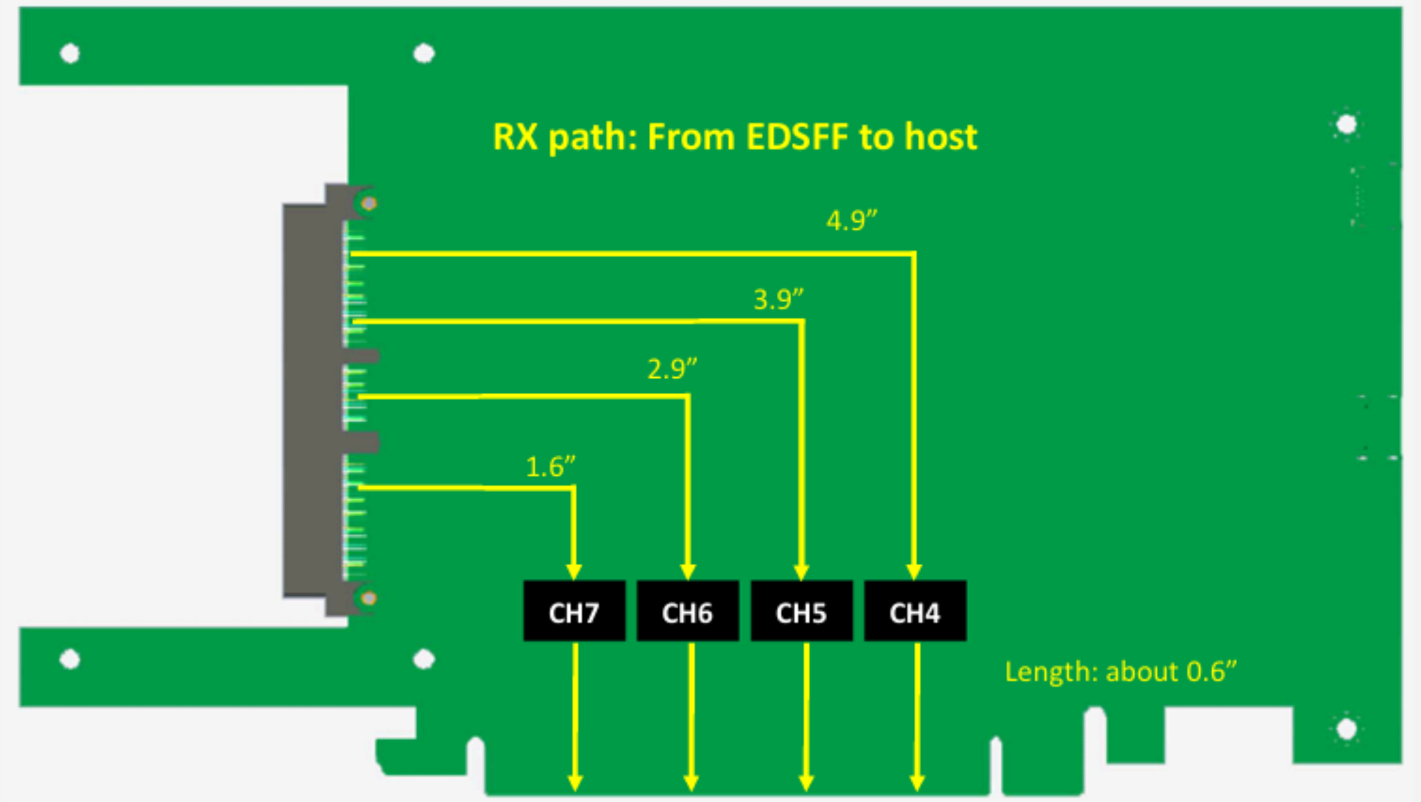


The redriver ICs are positioned approximately 1 inch from the host-side reference to support mid-channel signal conditioning.

RX Path – From EDSFF to Host

Channels CH4 through CH7 are routed with trace lengths optimized for reverse-direction signaling.

- **CH4** – 4.9 inches
- **CH5** – 3.9 inches
- **CH6** – 2.9 inches
- **CH7** – 1.6 inches

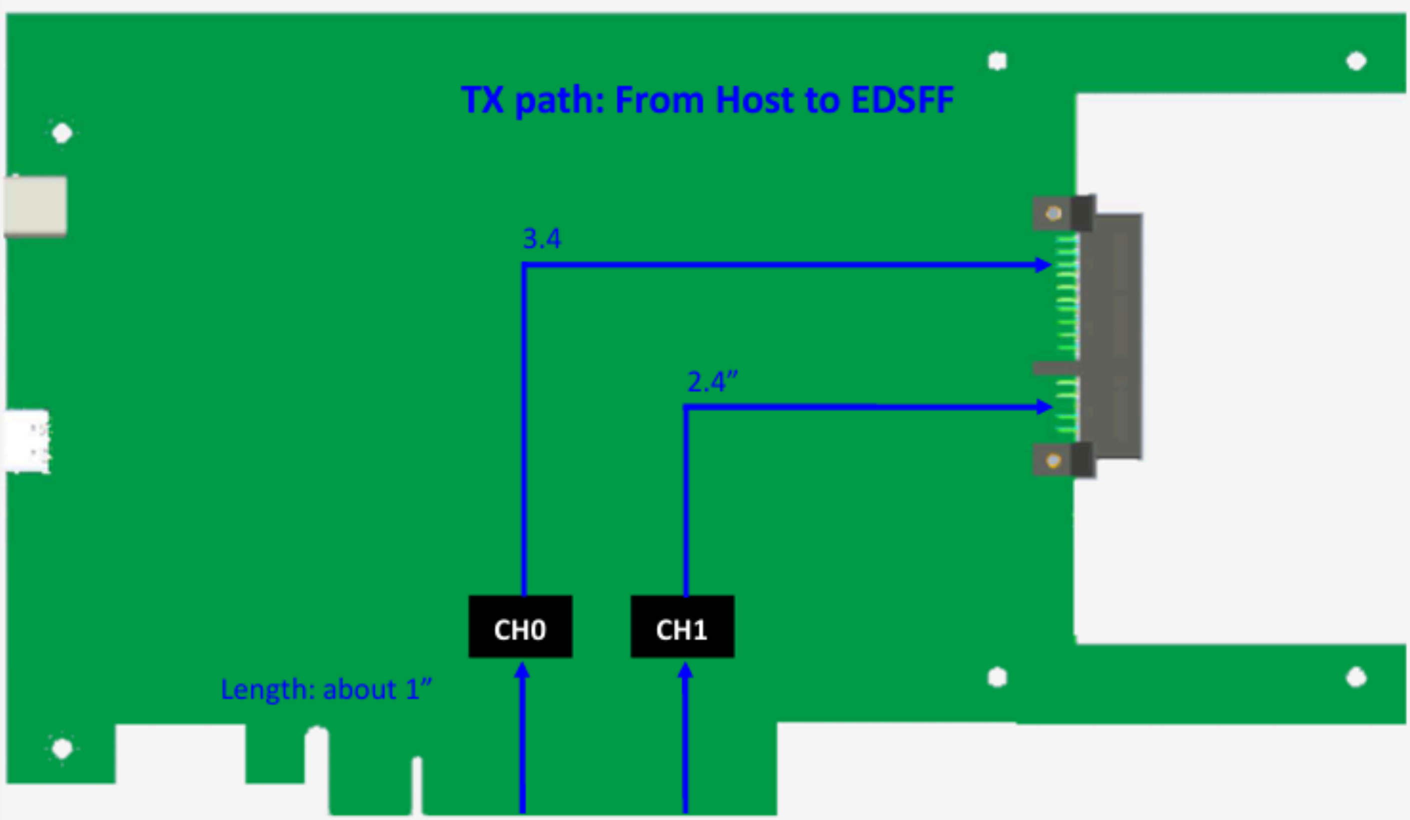


The receive-side routing places the redriver ICs approximately 0.6 inches from the connector to minimize insertion loss prior to signal conditioning.

TX Path – From Host to EDSFF

Channels CH0 and CH1 are routed through dedicated redriver ICs positioned near the host interface.

- **CH0** – 3.4 inches
- **CH1** – 2.4 inches

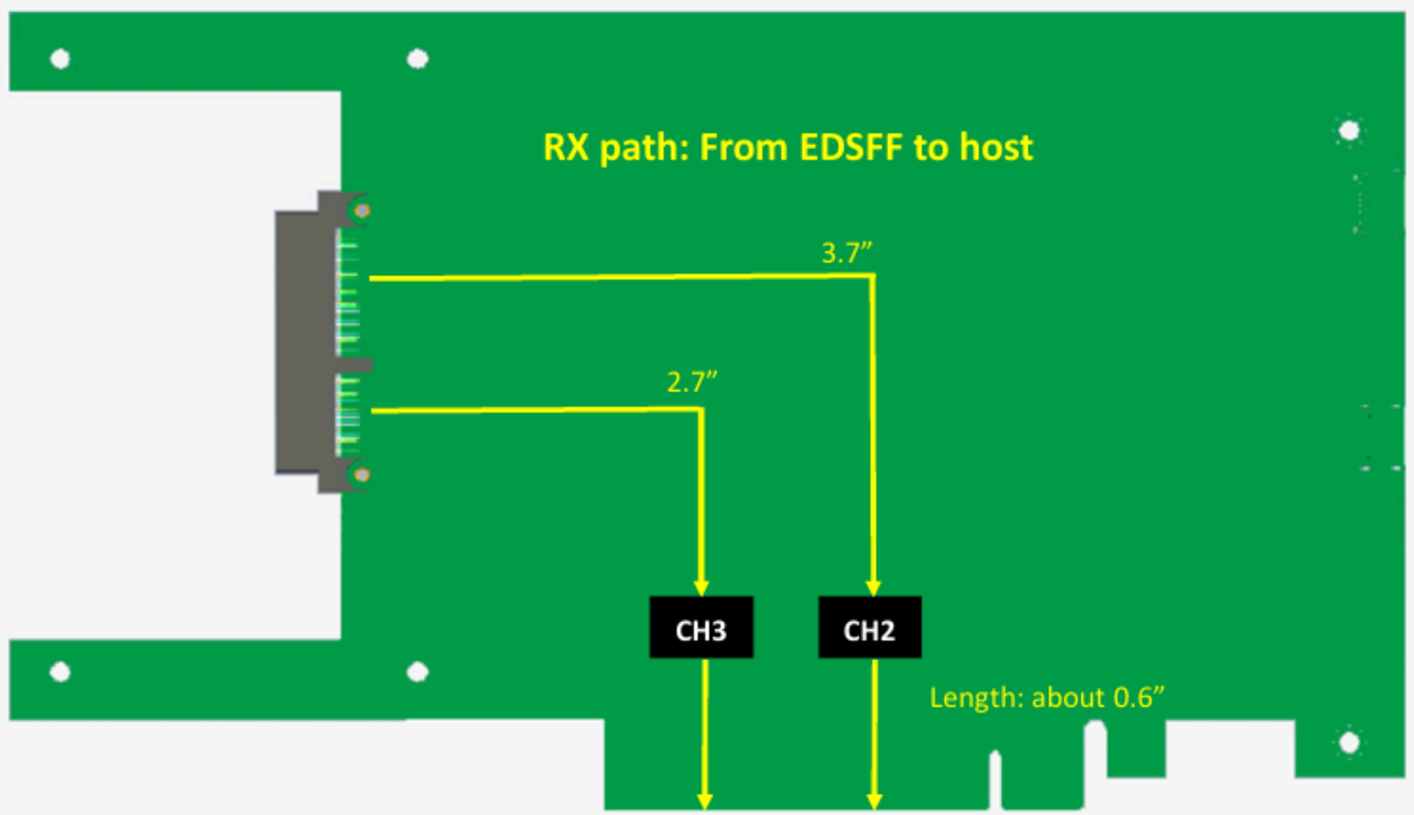


The redriver ICs are positioned approximately 1 inch from the host-side reference to support mid-channel signal conditioning.

RX Path – From EDSFF to Host

Channels CH2 and CH3 are routed from the EDSFF connector toward the host with optimized trace lengths.

- **CH2** – 3.7 inches
- **CH3** – 2.7 inches



The redriver ICs are positioned approximately 0.6 inches from the connector to preserve signal quality before conditioning.

Installing SSDs

The PCIe Gen6 Redriver Adapter supports multiple EDSFF and enterprise SSD form factors using dedicated trays, holders, and block-plates. Each assembly adapts the SSD for use with the redriver and fan cage to maintain proper mechanical alignment and airflow.

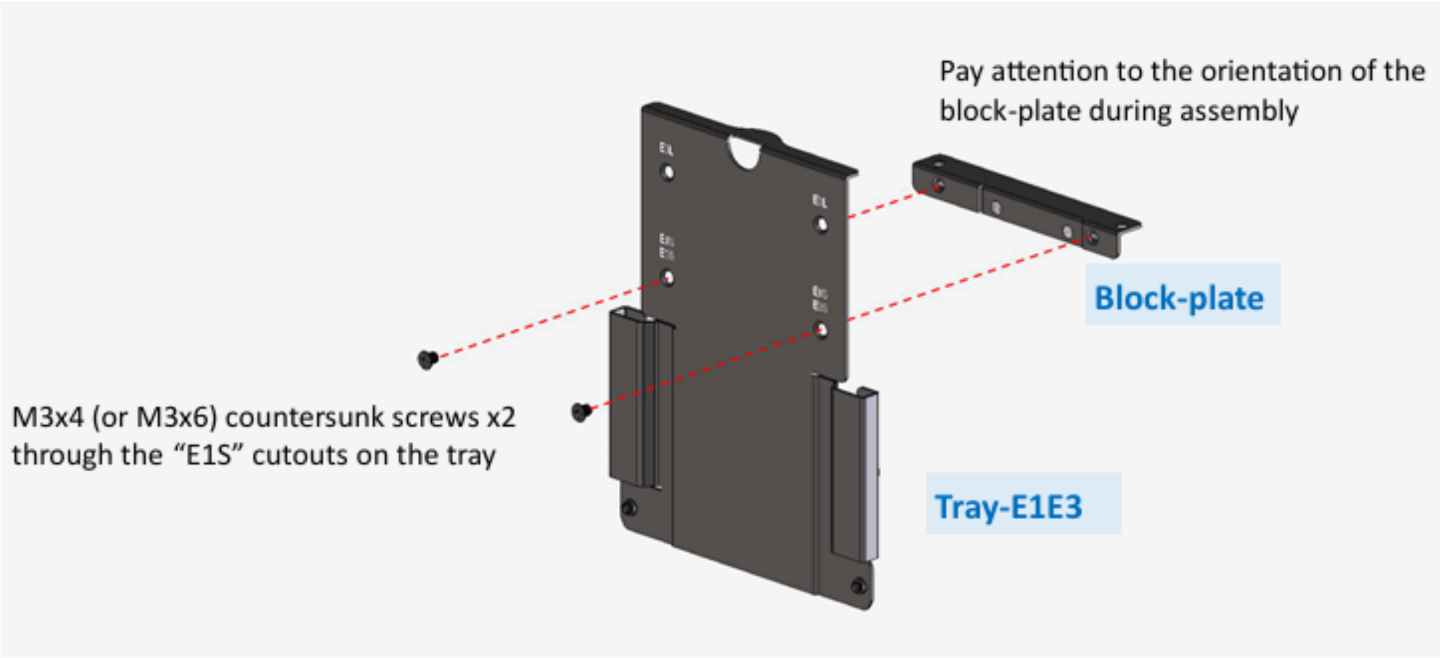
Before installation, power off the system, disconnect all power sources, and handle components in an ESD-safe environment. Verify that the correct tray, holder, and block-plate are selected for the target SSD type.

Select the appropriate SSD type to view installation instructions:

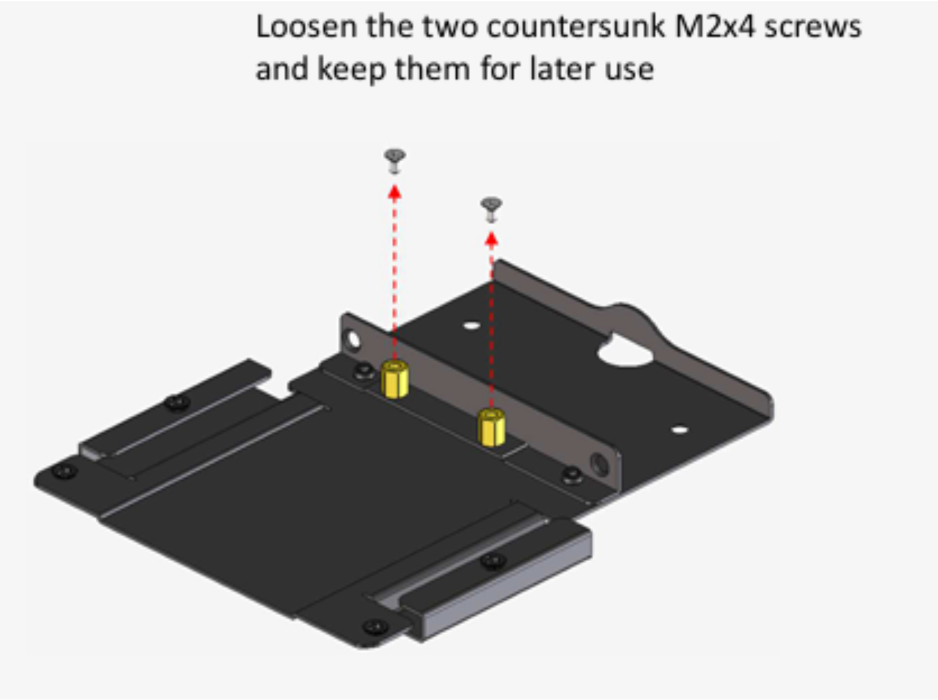
- **E1.S SSD**
- **E3.S / E3.L 1T SSDs**
- **E3.S / E3.L 2T SSDs**
- **E2 SSDs**

E1.S SSDs

1. Mount the block-plate on the tray. Secure the block-plate using **M3x4 or M3x6 (x2) countersunk screws** through the **E1.S cutouts** on the tray.



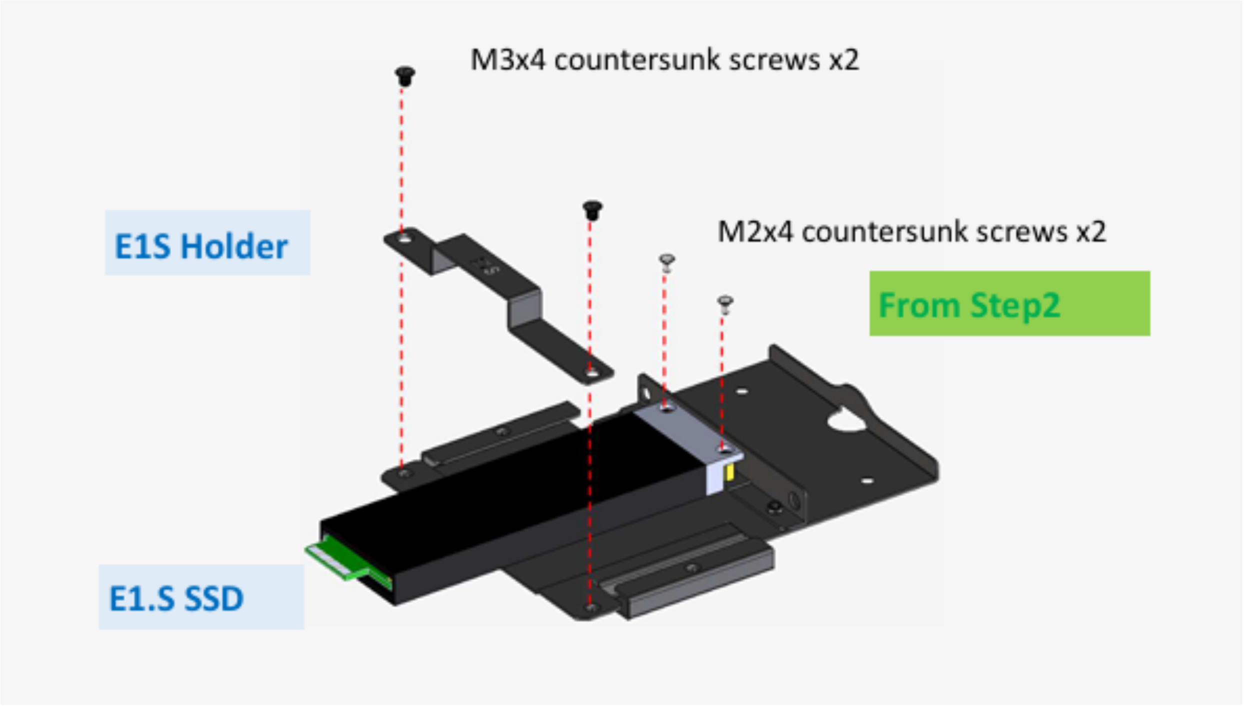
2. Loosen the **M2x4 (x2) countersunk screws** on the tray and retain them for later use.



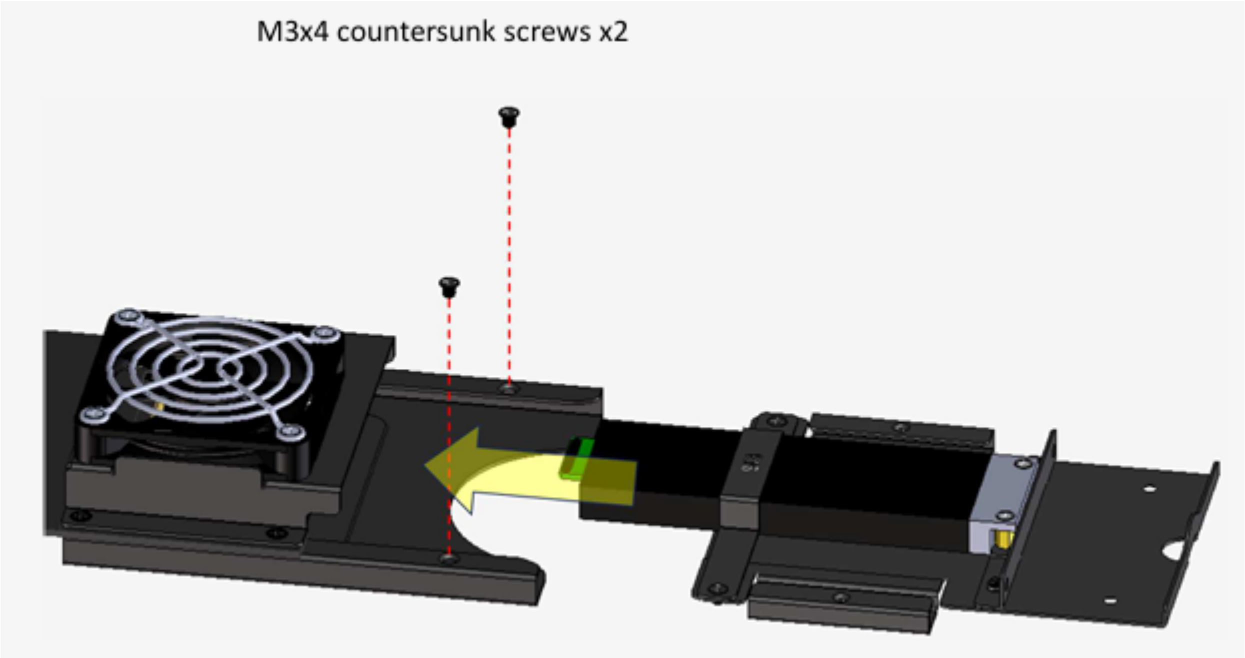
3. Place the E1.S SSD into the holder with the connector facing the rear.

4. Position the holder over the SSD and secure it using **M3x4 (x2) countersunk screws**.

5. Reinstall the **M2x4 (x2) countersunk screws** loosened in step 2.

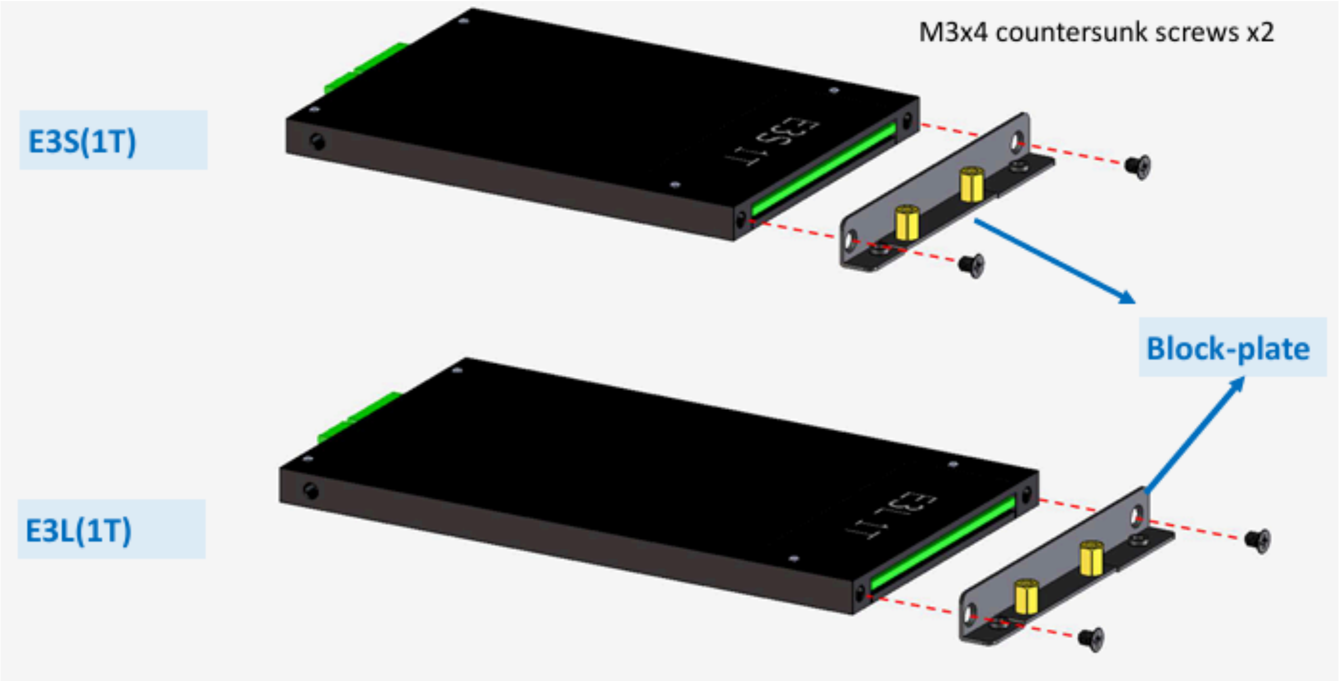


6. Insert the assembled SSD tray into the fan cage and fasten it using **M3x4 (x2) countersunk screws**.

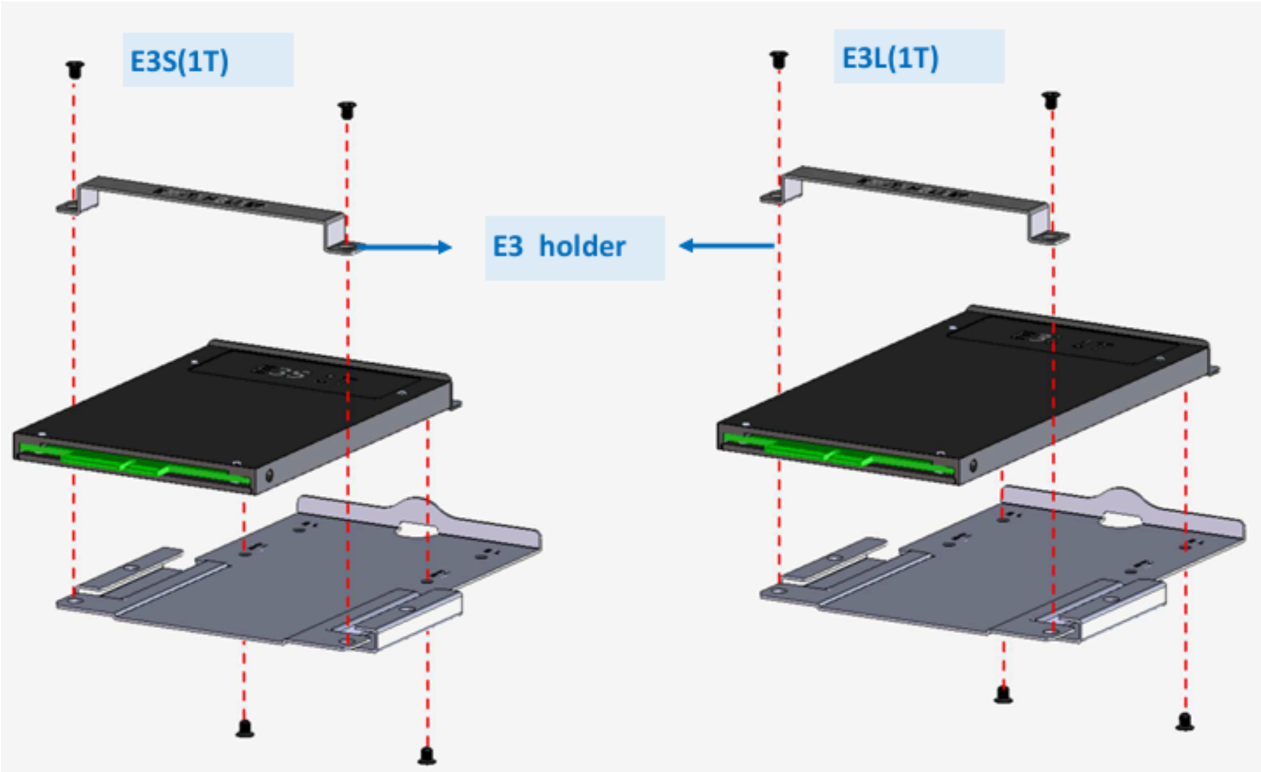


E3.S / E3.L 1T SSDs

1. Mount the block-plate on the rear of the SSD using **M3x4 (x2) countersunk screws.**

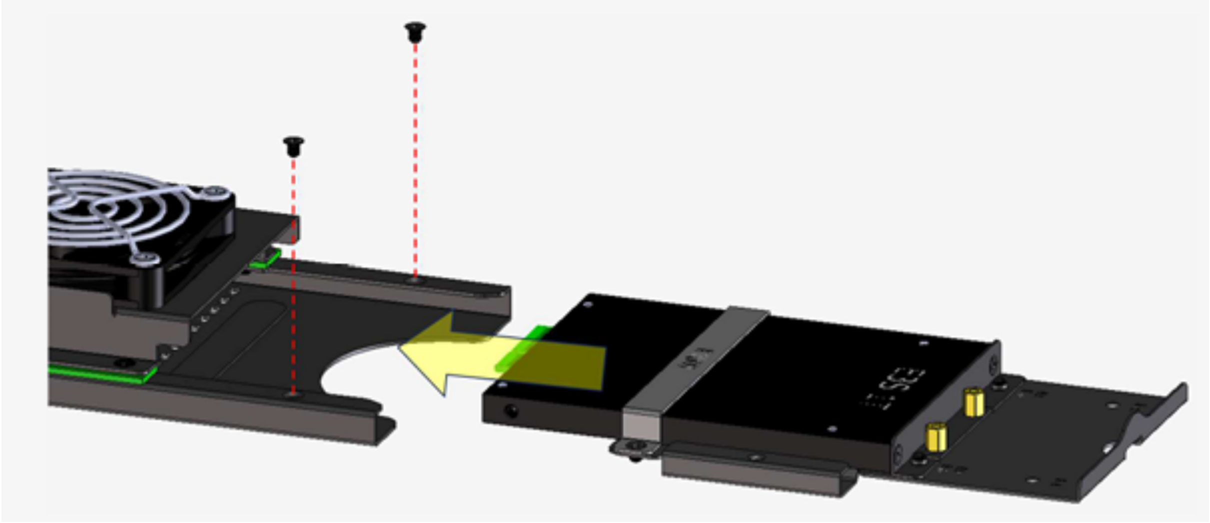


2. Place the SSD onto the tray and install the E3 holder over the top. Secure the SSD to the tray using **M3x4 or M3x6 (x2) countersunk screws** through the E3.S or E3.L cutouts.



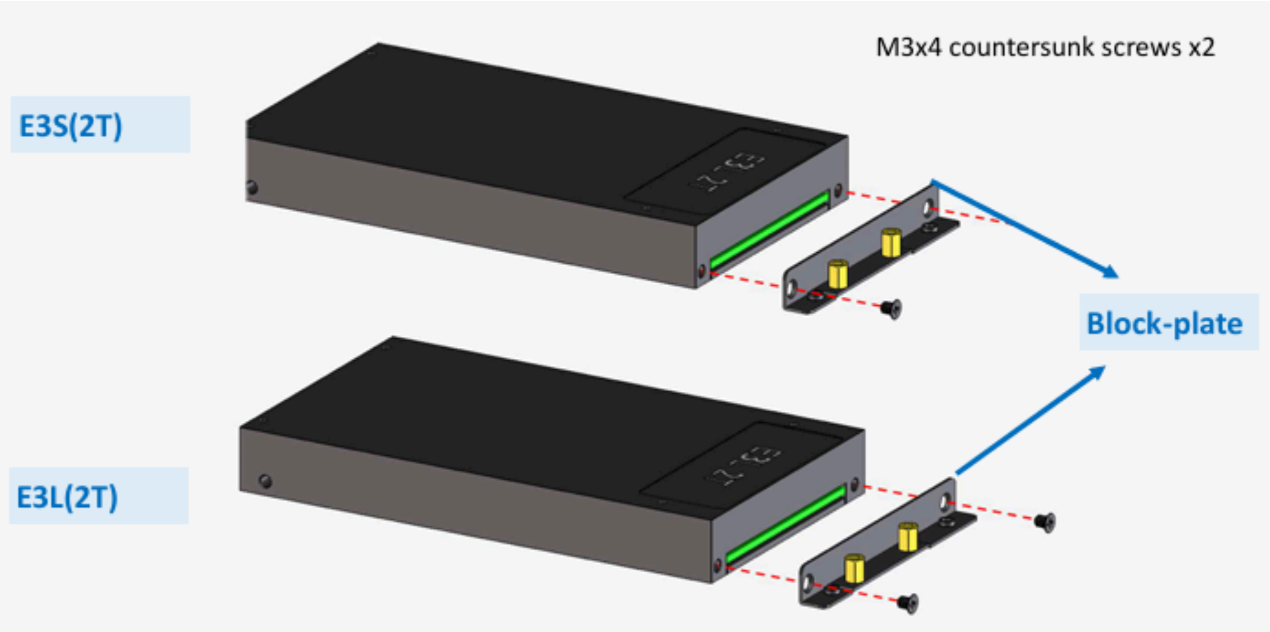
M3x4 (or M3x6) countersunk screws x2 through the "**E3S**" or "**E3L**" cutouts on the tray

3. Insert the assembled tray into the fan cage and secure it with **M3x4 (x2) countersunk screws**.

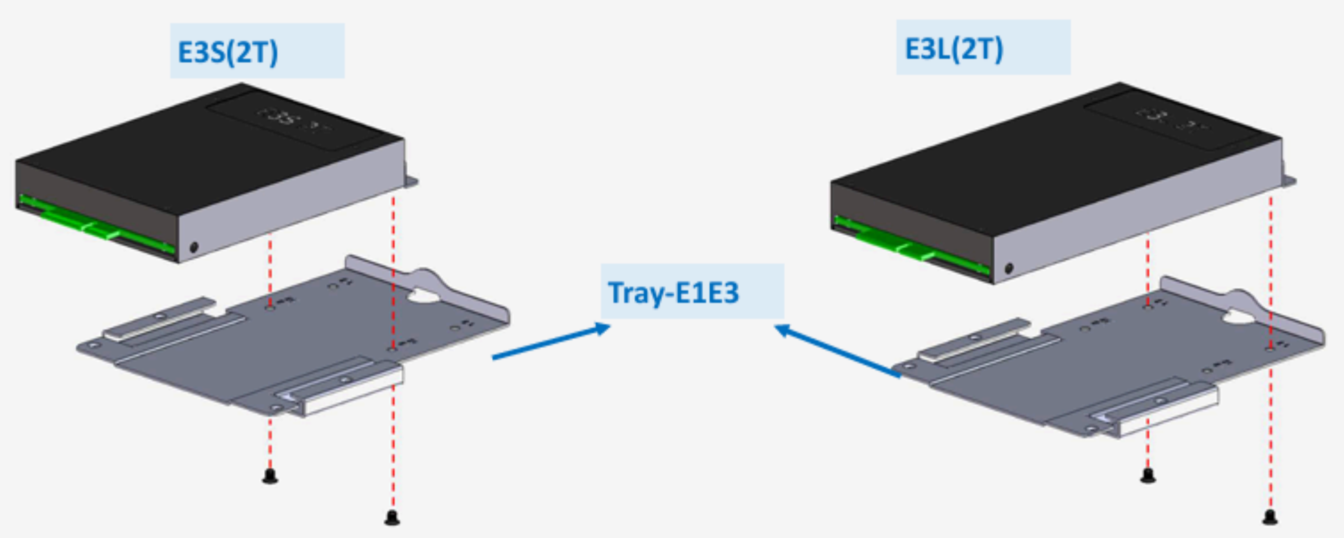


E3.S / E3.L 2T SSDs

1. Mount the block-plate on the rear of the SSD using **M3x4 (x2) countersunk screws**.

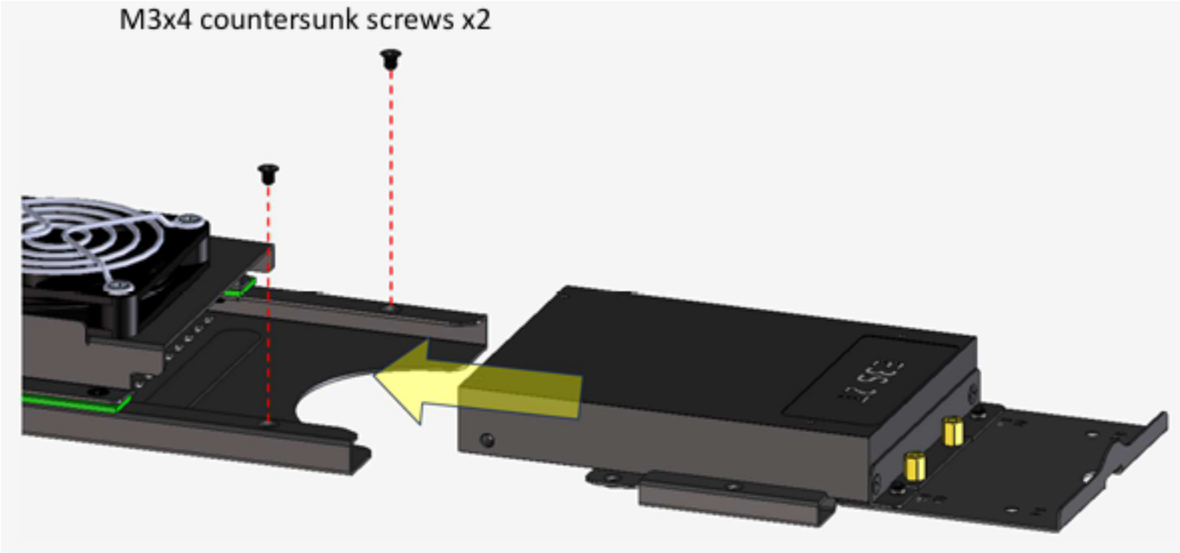


2. Place the SSD onto the Tray-E1E3 and align the mounting holes. Secure the SSD to the tray using **M3x4 or M3x6 (x2) countersunk screws** through the E3.S or E3.L cutouts.



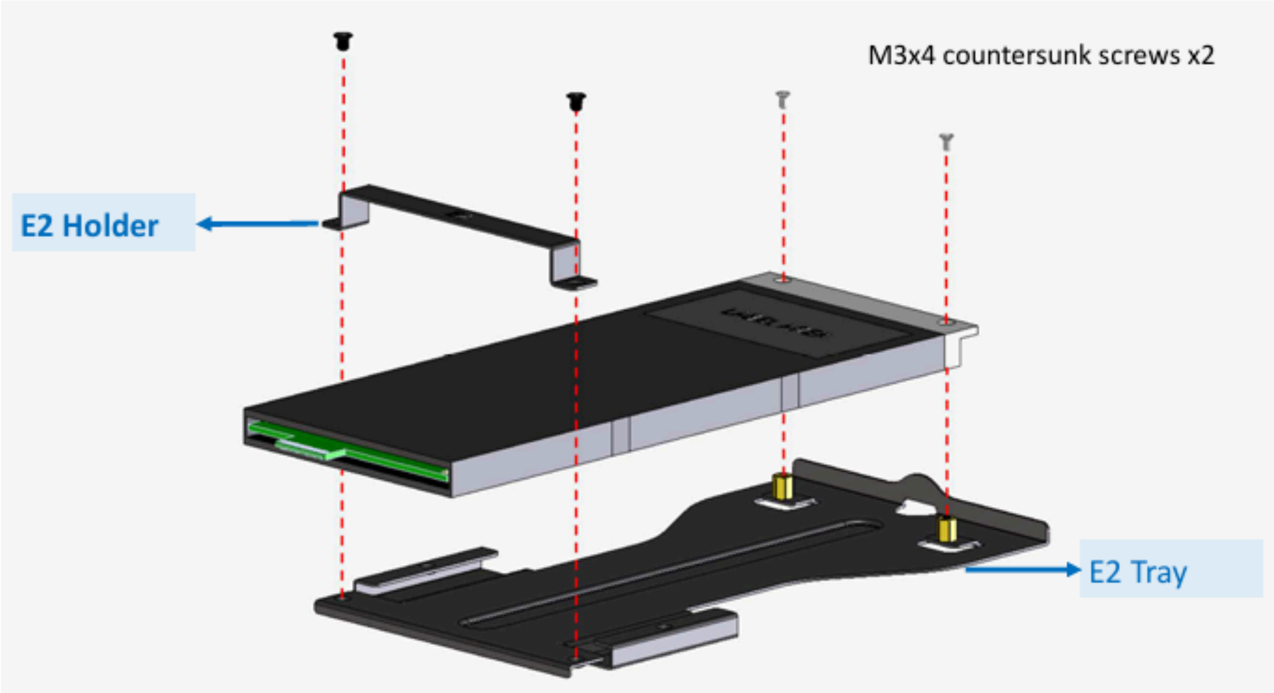
M3x4 (or M3x6) countersunk screws x2 through the "**E3S**" or "**E3L**" cutouts on the tray

3. Insert the assembled tray into the fan cage and fasten it using **M3x4 (x2) countersunk screws**.



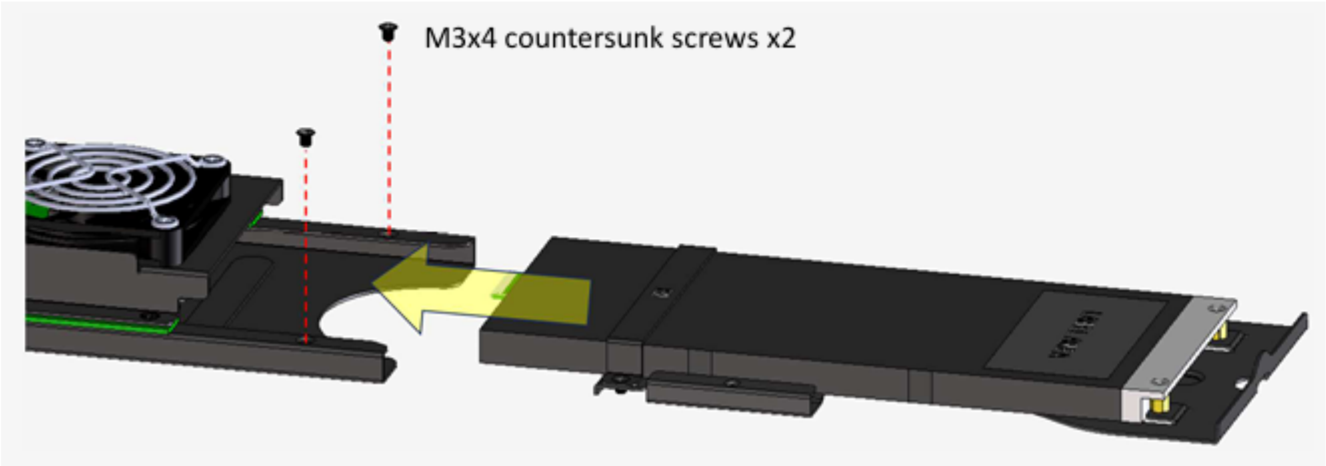
E2 SSDs

1. Place the E2 SSD onto the E2 tray. Install the E2 holder over the SSD and secure it using **M3x4 (x2) countersunk screws**.



S

2. Insert the assembled SSD tray into the fan cage and fasten it using **M3x4 (x2) countersunk screws**.



MCU Command Reference

Commands	Description
help	Display all available commands
fdl	Upgrade MCU firmware via XMODEM
lsd	Shows board temperature and current.
eq	Configure PS7161 receiver equalization
fg	Configure PS7161 receiver flat gain
sw	Configure PS7161 transmitter swing
tune	Step-by-step EQ, gain, and swing tuning
load	Load default EQ, gain, and swing settings
save	Save current EQ, gain, and swing to all channels
perst	Assert PERST# to EDSFF for 30 ms
dual	Enable or disable EDSFF dual-port mode
pwrdis	Set EDSFF PWRDIS pin level high or low
hled	Control EDSFF host (amber) LED
detect	Control EDSFF host LEDs
bist	Run on-board device diagnostics
iicwr	Run on-board device diagnostics
iicw	Read SMBus data from slot devices
ver	Display part number, serial number, and MCU firmware information
sysinfo	Show complete system summary
reset	Reset the MCU firmware

Command Usage Notes

Firmware Upgrade — fdl

Initiates MCU firmware upgrades via XMODEM transfer. After running the command, the MCU waits for incoming data from the terminal software.

To upgrade firmware:

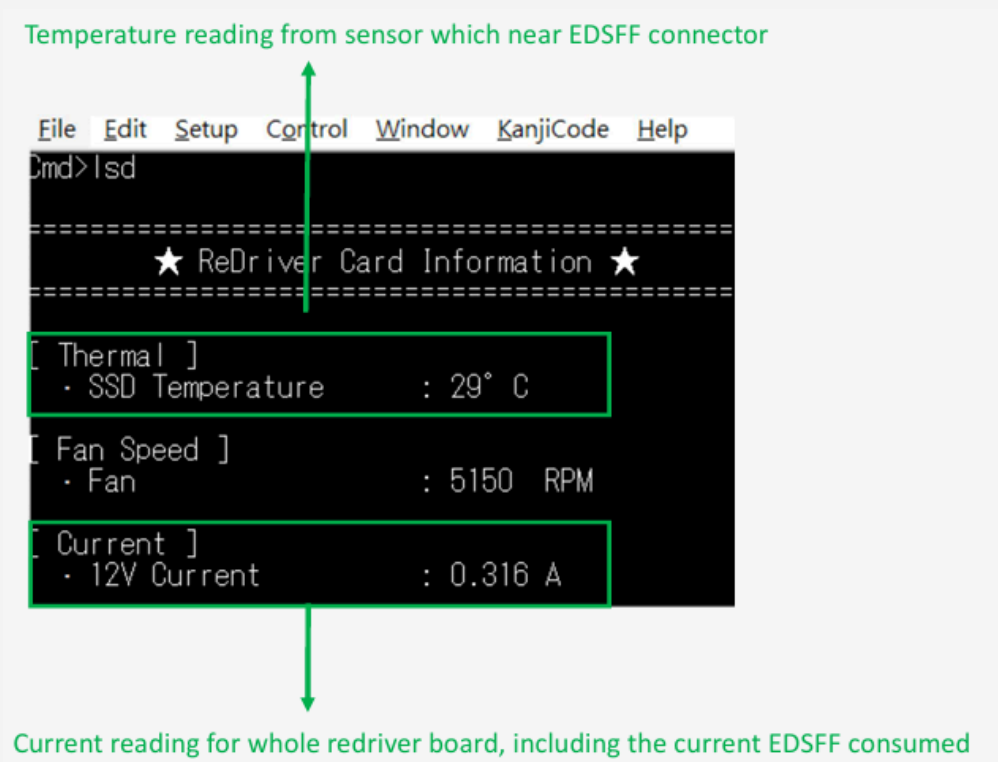
1. Type **fdl mcu** at the CLI prompt.
2. In the terminal application, select **Transfer** → **Send File**.
3. Set **Protocol: XMODEM**, then start the transfer.

The update typically completes within a few seconds.

Maintain a stable USB connection during the transfer. Power interruptions or serial disconnects may corrupt the firmware image.

System Status — lsd

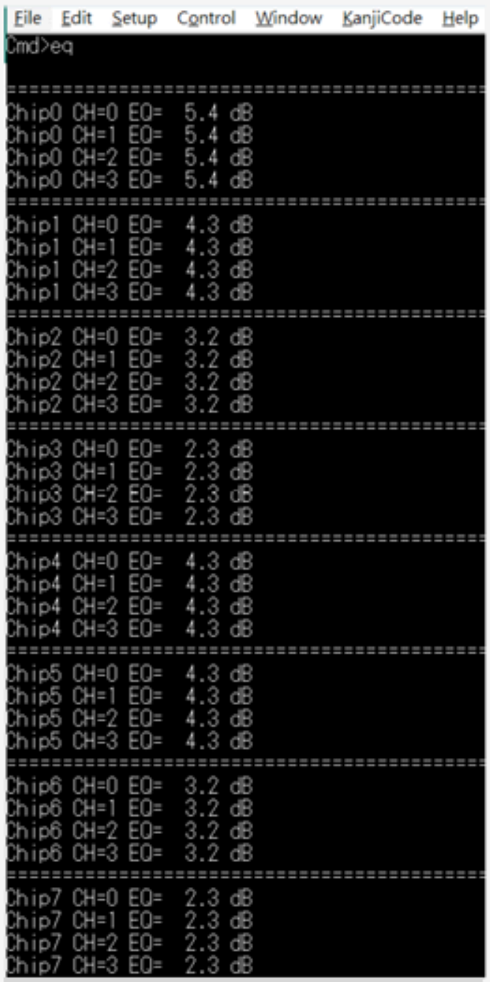
The **lsd** command displays real-time board temperature and current measurements collected by the on-board sensors. The output of this command will appear as follows:



Receiver Equalization — eq

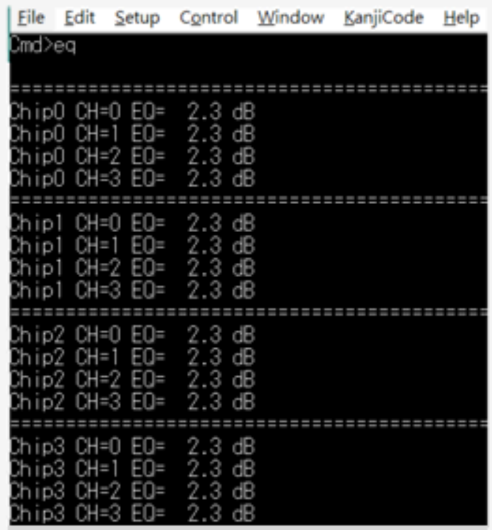
Configures the receiver equalization (EQ) settings of the PS7161 redriver ICs. This command is used to compensate for channel loss on the receive path.

If the **eq** command is entered without parameters, the CLI displays the current EQ settings for the entire card, including chip index, channel, and EQ value.



Show all EQ setting for

X16 EDSFF Redriver card



Show all EQ setting for

X8 EDSFF Redriver card

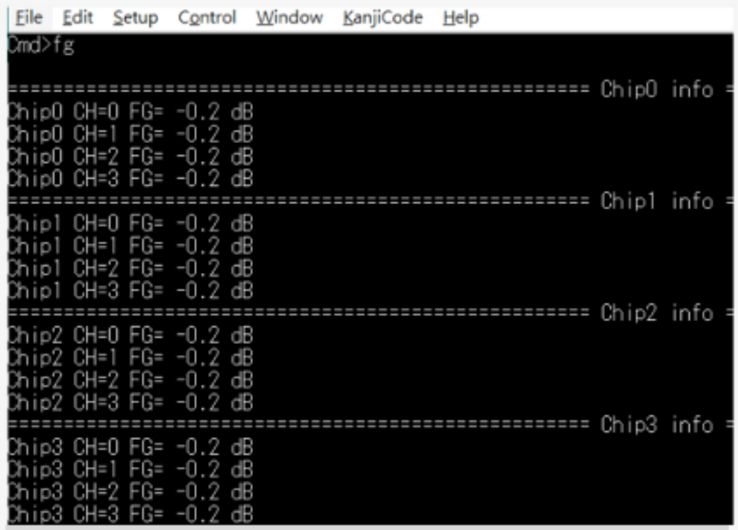
Enter the command **eq** followed by the chip number (x16: 0–7, x8: 0–3) or **`all`**, and the EQ value (0–15) to configure PS7161 receiver equalization. For example:

- **eq all 1** — Sets EQ value 1 on all PS7161 redriver chips
- **eq 0 3** — Sets EQ value 3 on chip 0
- **eq 2 5** — Sets EQ value 5 on chip 2

Receiver Flat Gain — fg

Configures the receiver flat gain setting of the PS7161 redriver ICs. Flat gain controls overall signal amplification on the receive path.

If the **`fg`** command is **entered without parameters**, the CLI displays the current flat gain settings for the entire card, including chip index, channel, and gain value.



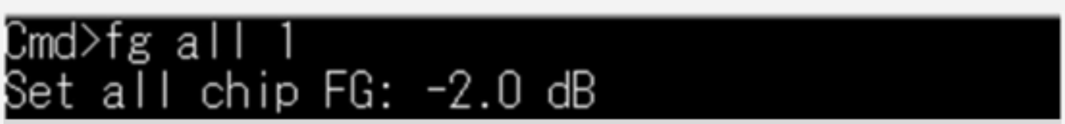
Show all flat gain setting for

X8 EDSFF Redriver card

Enter the command **`fg`** followed by the chip number (x16: 0–7, x8: 0–3) or **`all`**, and the flat gain value (0–3).

For example:

- **`fg all 1`** — Sets flat gain value 1 on all PS7161 redriver chips
- **`fg 0 2`** — Sets flat gain value 2 on chip 0
- **`fg 3 0`** — Sets flat gain value 0 on chip 3



Transmitter Swing — sw

Configures the transmitter output swing setting of the PS7161 redriver ICs. Swing controls the amplitude of the transmitted signal on the transmit path.

If the **sw** command is **entered without parameters**, the CLI displays the current transmitter swing settings for the entire card, including chip index, channel, and swing value.

S

Enter the command **sw** followed by the chip number (x16: 0–7, x8: 0–3) or **all**, and the swing value (0-7).

For example:

- `sw all 2` — Sets transmitter swing value 2 on all PS7161 redriver chips
- **sw 1 3** — Sets transmitter swing value 3 on chip 1
- **sw 5 1** — Sets transmitter swing value 1 on chip 5

Automatic Tuning — tune

Performs step-by-step tuning of receiver equalization, flat gain, and transmitter swing on the PS7161 redriver ICs. Just enter the command **`tune`** to start the guided tuning process.

Follow the on-screen prompts to adjust EQ, flat gain, and swing values in one go:

```
Cmd>tune

1. Please enter chip ID (0-7), or type 'q' to quit. :0

2. Please enter channel ID (0-3), or type 'q' to quit. :0

3. Please enter eq value (0-15), or type 'q' to quit. :0

4. Please enter fg value (0-3), or type 'q' to quit. :0

5. Please enter sw value (0-7), or type 'q' to quit. :0

Chip0, CH:0, EQ:  2.3 dB, FG: -2.8 dB, SW: 1050 mv
```

Load Predefined Configurations — load

Loads a predefined default configuration for the PS7161 redriver ICs. Default configurations are optimized for different trace-length ranges. The available modes are:

- **s (Short)** – For host-to-slot trace lengths under 9 inches
- **m (Medium)** – For host-to-slot trace lengths around 6–9 inches (factory default)
- **l (Long)** – For host-to-slot trace lengths over 10 inches, up to ~12 inches

To select a specific configuration, enter **`load`** followed by **`s`**, **`m`**, or **`l`**. For example:

- **load** — Displays the default configuration currently set for boot
- **load m** — Loads the Medium default configuration

```
Cmd>load m

Ready to load 'Medium' configuration into PS1761.
Confirm? (Press 'y' to continue, any other key to abort):y

Successfully loaded 'Medium' configuration.
```

Save Current Configuration — save

Saves the current EQ, flat gain, and transmitter swing settings applied to the PS7161 redriver ICs. Use the **save** command after manual tuning or after modifying default profiles to preserve the current configuration.

```
Cmd>save

Save configuration
Yes[y/Y] or Any key quit?y

Save configuration Success.
```

The newly saved settings are retained in non-volatile memory and are automatically applied the next time the redriver card powers on or resets.

PERST# Control – perst

Asserts the PERST# (PCIe reset) signal to the connected EDSFF device. This command is typically used to recover a device after link training issues, configuration changes, or error conditions without removing power from the system.

Enter the command **perst** followed by the target channel (**a** or **b**) to issue a reset pulse. The PERST# signal is asserted for approximately 30 ms and then released automatically.

- **perst** – Resets both channels
- **perst a** – Resets channel a

```
Cmd>perst a
Reset channel a of E3 success
```

Dual-Port Control — dual

Controls whether an attached EDSFF device operates in single-port or dual-port mode. Dual-port mode allows an EDSFF SSD to expose two independent PCIe ports. This command drives the EDSFF **Dual Port Enable# signal (Pin B9)**.

Enter the command `dual` followed by **on** or `off` to change the setting. For example:

- **dual** — Displays the current EDSFF dual-port status
- **dual on** — Enables dual-port operation on the attached EDSFF device
- **dual off** — Forces single-port operation

Power Disable Control — pwrdis

Controls the **Power Disable (PWRDIS)** signal on **EDSFF Pin 3**, which determines whether the attached EDSFF device is allowed to power on. When PWRDIS is asserted, the SSD remains electrically present but is prevented from powering up. This is commonly used for controlled power sequencing or service operations.

Enter the command `pwrdis` followed by **h** or **l** to set the PWRDIS signal level.

For example:

- **pwrdis h** — Disables EDSFF device power.
- **pwrdis l** — Enables EDSFF device power.

Host LED Control – hled

Controls the **host-driven LED signal** on the attached EDSFF device. This command toggles the **amber host LED**, which is typically used to indicate host-defined status such as identification or service conditions.

Enter the command `hled` followed by **on** or **off** to control the host LED state.

For example:

- **hled on**— Turns the EDSFF host (amber) LED on
- **hled off** — Turns the EDSFF host (amber) LED off

Amber
Host (LED signal)
Host defined
585 to 600
Minimum[2]: 40

Presence Detection – detect

Displays the presence and link width of the attached EDSFF device. This command reports the detected PCIe lane width based on the EDSFF presence signals.

Enter the command **`detect`** to query the current EDSFF device status. The CLI reports whether the attached EDSFF device is detected as x4, x8, or x16.

```
Cmd>detect

E3 present detection: X4
Cmd>detect

E3 present detection: X8
```

Built-In Self-Test — bist

Runs built-in self-tests on the redriver card to verify basic hardware and communication functionality.

If any component fails, the CLI will report **Fail**:

Channel	Device	Address	Status
CH0	PS7161-1	0x3A	OK
CH1	PS7161-2	0x5A	OK
CH1	PS7161-3	0x62	OK
CH1	PS7161-4	0x64	Fail
CH1	PS7161-5	0x8E	OK

```
Cmd>bist

Channel   Device      Address    Status
---------------------------------------------
CH0       PS7161-1    0x3A       OK
CH0       PS7161-2    0x5A       OK
CH0       PS7161-5    0x8E       OK
CH0       PS7161-6    0x6E       OK
CH1       PCA9575     0x42       OK
CH1       AT24C64     0xA0       OK
```

SMBus Read — iicwr

Reads SMBus data from devices attached through the EDSFF connector. This command is typically used to access device registers for diagnostics or validation.

Enter **iicwr** followed by the device address (hex), read length (1–128), and the starting register offset (hex). The maximum number of bytes that can be read in a single command is 128 bytes.

For example:

- **iicwr d4 8 0** – Reads 8 bytes from SMBus device address 0xd4, starting at register 0x00

```
Cmd>iicwr d4 8 0

Data [0] = 6
Data [1] = bb
Data [2] = ff
Data [3] = 1c
Data [4] = 0
Data [5] = 4d
Data [6] = 19
Data [7] = e
```

SMBus Write — iicw

Writes SMBus data to devices attached through the EDSFF connector. This command is typically used to write register values or configuration data to an attached EDSFF device.

Enter the command **iicw** followed by the device address (hex) and one or more data bytes (hex) to be written. For example:

- **iicw d4 ff** – Writes 0xFF to the device at address 0xd4

```
Cmd>iicw d4 ff

Write Data [0] = ff
```

System Version — ver

Displays product name, serial number, MCU firmware version, and build information. Use this command to verify firmware version before upgrades or troubleshooting.

---------- Product Info -----------	
Company :	Serial Cables
Model :	GEN6 E3 HOR REDRIVER
Serial No. :	R6PE3251201002
---------- App Info -------------	
Version :	0.0.3
Build Time :	Aug 7 2025 14:39:36

System Information — sysinfo

Displays detailed system information for the redriver card, including:

- Company name, model, and serial number
- Firmware version and build time
- SSD temperature
- Fan speed (RPM)
- 12V current measurement
- Detected devices, SMBus addresses, and health status per channel

This is effectively a sequence of several key commands (**ver**, **lsd**, **bist**), consolidated into a single report for quick system validation.

System Reset — reset

Resets the on-board MCU firmware without affecting the redriver ICs or the attached EDSFF device.

Use **reset** after configuration changes, firmware updates, or if the CLI becomes unresponsive. .

Maintenance & Diagnostics

The redriver card provides built-in CLI commands for monitoring system health and diagnosing issues at the device and board level. Regular checks help catch thermal, power, or device problems early.

- Run **lsd** to verify board temperature and current readings during normal operation.
- Use **sysinfo** before and after maintenance to review firmware version, fan speed, power status, and redriver device health.
- After changing tuning parameters or loading a new default profile, use **eq**, **fg**, or **sw** (without arguments) to confirm current settings across all chips and channels.
- If an attached EDSFF device fails to link or enumerate correctly, run `detect` to verify lane width and `perst` to reinitialize the device.

Revision History

Revision	Description
1.3	Updated cover and disclaimers
1.2	Reformatted and restyled for brand consistency and readability. Rewritten for clarity. Added *Product Overview, Safety, Handling & Compliance*, *Maintenance & Diagnostics*, and *Contact Us* sections.
1.0	Initial manual release.

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